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# Design of A Series-Loaded Resonant DC-DC Converter with Clamped Voltage (SLCCV)

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***Abstract:*** *Theoretical and experimental results of a SLCCV operating above 200 kHz are presented. Circuit waveforms, small-signal model and large signal model are given. Finally a complete scheme of a switch-mode power supply built around a Series - Loaded Resonant Converter With Clamped Voltage is also given. The DC voltage for power stage is around 350V and it is provided by a power factor correction preregulator from mains (220 Vrms AC).*
***Keywords:*** *Series-resonant/converter/clamped voltage..*

## I. INTRODUCTION

Recently the resonant converter has been given a great deal of attention by both industry and academia [1..10]. Many different topologies exist, and new configurations appear in the literature quite frequently.

On this moment, the resonant converters are defined as the combination of converter topologies and switching strategies that result in zero-voltage and/ or zero current- switching. One way to categorize DC-DC converters is as follows:

1. Load-resonant converters;
2. Resonant -switch converters.

These classification are explained further:

*Load -resonant converters* consists of an L-C resonant tank circuit. Oscillating voltage and current, due to L-C resonance in the tank, are applied to the load, and the converter switches can be switched at zero voltage and/ or zero current. Either a series L-C or a parallel L-C circuit can be used. In these converter circuits, the power flow to the load is controlled by the resonant tank impedance, which in turn is controlled by the switching frequency $f_s$ in comparison to the resonant frequency $f_R$ of the tank.

*Resonant -switch converters*; In certain switch-mode converter topologies, an L-C resonance can be utilized primarily to shape the switch voltage and current to provide zero voltage and /or zero current switching. In such resonant -switch converters, during one switching frequency period , there are resonant as well as nonresonant operating intervals. Therefore, in the literature, these converters have also been termed quasi-resonant converters.

## II. THEORETICAL CONSIDERATIONS

By considering a complete design for a specific application, the merits and the limitations of SLCCV can be more fully understood. Comparisons between predicted, simulated and measured performance verifies design and analysis tools that have been developed. This allows a designer to use these tools for a comparative analysis of different converters, and for detailed designed guidelines.

The topology of power stage is presented in Fig1. The circuit works at a switching frequency under resonance frequency. We will have two modes of operation. In mode II the diode D1 and D2 conduct, and this mode is important for DC-DC converter application. A detailed steady-state analysis of each mode will be done. Also for mode II , a small -signal model will be present.

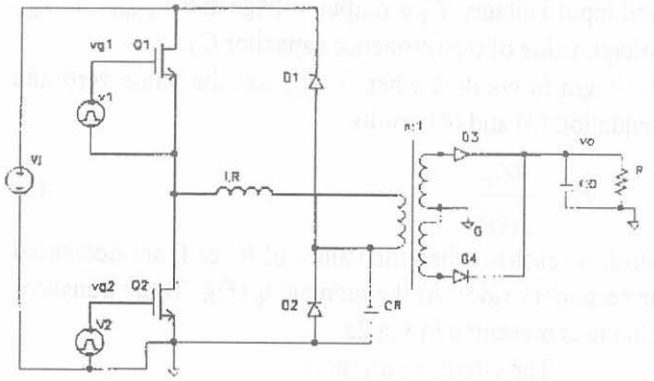


Fig. 1 *The power stage.*

The output capacitor, the load and the transformer are modeled by voltage source $nV_o$ whose polarity is determined by $D_3$ and $D_4$ conduction. Since the circuit's behavior is largely determined by values of $L_R$ and $C_R$ the following parameters are defined as:

1) characteristic impedance: $Z_R = \sqrt{\frac{L_R}{C_R}}$ ;

2) resonant angular frequency: $\omega_R = \frac{1}{\sqrt{L_R C_R}}$ ;

3) resonant period: $T_R = \frac{2\pi}{\omega_R}$ ;

4) switching period in the secondary side: $T_s$ ;

5) duty factor: $\delta = \frac{T_R}{2T_s}$ .

Assuming losses are negligible, the input power equals the output power. Starting from this assumption the following equations can be demonstrate for mode I of operation:

$$I_I = \frac{I_o}{2n} \qquad (1)$$

$$V_o = \frac{V_I}{2n} \tag{2}$$

$$V_{CR\min} = \frac{V_I}{2} - \frac{\pi V_I Z_R}{4\delta R n^2} \tag{3}$$

$$V_{CR\max} = \frac{V_I}{2} + \frac{\pi V_I Z_R}{4\delta R n^2} \tag{4}$$

where $I_I$, $V_I$ are input current and input voltage, $V_O$ is output voltage and $V_{CRmin}$ , $V_{CRmax}$ are minimum and maximum voltage value of the resonance capacitor $C_R$.

The diodes $D_1$ and $D_2$ begin to conduct when $V_{CRmin}$ has the value zero and $V_{CRmax}$ has the value $V_I$. From equation (3) and (4) results:

$$R \le \frac{\pi Z_R}{2\delta n^2} \tag{5}$$

The Mode II of operation is reached when the values of R or $f_s$ are decreased ($f_s$ is switching frequency in the secondary side). At the moment $t_0$ (Fig. 3) the transistor $Q_1$ conducts. The equivalent scheme is presented in Fig.2a.

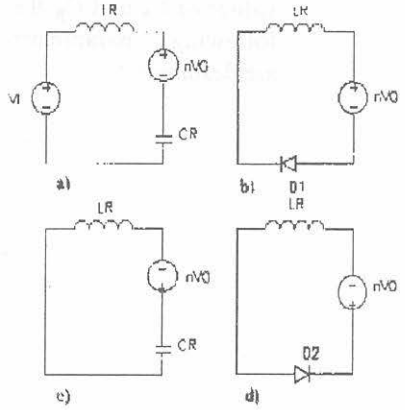


Fig. 2 *The equivalent schemes.*

The circuit's current is:

$$i_{LR}(t) = \frac{V_I - nV_o}{Z_R} \sin \omega_R (t - t_0) \tag{6}$$

At the moment $t_1$, the capacitor $C_R$ charges to $V_I$ and diode $D_1$ begin to conduct (the equivalent scheme is shown in Fig.2b). The current expression is:

$$i_{LR}(t) = i_{LR}(t_1) - \frac{nV_O}{L_R}(t - t_1) \tag{7}$$

At time $t_2$ the circuit's current reaches the zero value, the capacitor $C_R$ will be charged at the maximum value $V_I$.

At time $t_3$ the transistor $Q_2$ begin to conduct. The equivalent scheme is presented in Fig. 2c. The current will be:

$$i_{LR}(t) = -\frac{V_I - nV_O}{Z_R} \sin \omega_R (t - t_3) \tag{8}$$

At time $t_4$ the voltage across $C_R$ is zero. The diode $D_2$ is open and the circuit current has the value:

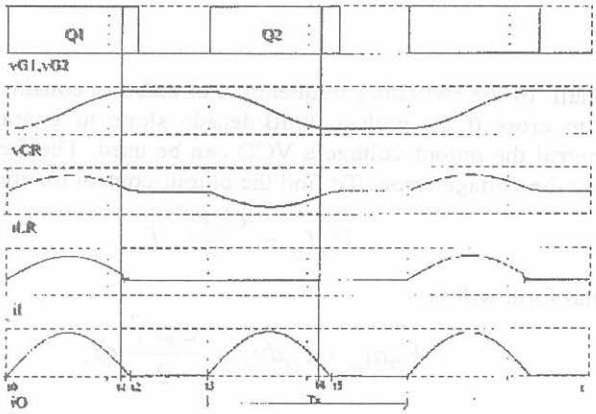


Fig. 3 *The specific waveforms.*

$$i_{LR}(t) = -i_{LR}(t_4) + \frac{nV_O}{L_R}(t - t_4) \tag{9}$$

The energy stored by $C_R$ at the moment $t_3$ is :

$$W = \frac{C_R V_I^2}{2} \tag{10}$$

This energy will be delivered to the load during $Q_2$ conduction. Due to the circuit symmetry, the energy delivered to the secondary during $Q_1$ conduction equals the energy delivered during $Q_2$ conduction. The energy delivered to the load can be written in terms of the output voltage and load current:

$$\frac{C_R V_I^2}{2} = V_O I_O T_S \tag{11}$$

Because $I_O = V_O / R$ the equation (11) becomes:

$$V_O = V_I \sqrt{\frac{C_R R}{2T_S}} \tag{12}$$

The equation (12) suggests that the output voltage can be maintained constant if the switching frequency is varied when the load and input voltage are modified.

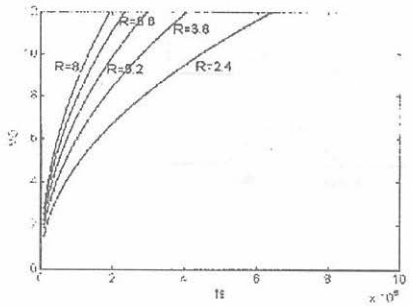


Fig. 4 *Output voltage Vo versus fs*

The Fig. 4 presents the output voltage versus $f_s$ for different value of the load.

## THE SMALL SIGNAL MODEL

Since regulation is maintained by feedback control, the loop gain of the system must be known in order to predict the power converter's performance. Tight d.c. regulation requires high loop gain. Good transient load response suppose a large bandwidth with the upper limit being

less then the half of the switching frequency. For stability considerations it is desirable for the gain to cross 0 dB with a 20dB/decade slope to guarantee adequate phase margin.To control the output voltage a VCO can be used. The frequency of VCO will be modified by the voltage error . To find the output-control function we start from:

$$V_O I_O = \frac{C_R V_I^2}{2} f_s \tag{13}$$

The differential form will be:

$$V_O di_o + I_O dv_o = \frac{C_R V_I^2}{2} df_s \tag{14}$$

but:

$$dv_o = di_o (R // \frac{1}{sC_o}) \text{ and } I_O = V_O / R \tag{15}$$

hence:

$$\frac{dv_o}{df_s} = \frac{V_I}{2} \sqrt{\frac{C_R R}{2 f_s}} \frac{1}{1 + \frac{sC_O R}{2}} \tag{16}$$

After the open loop transfer function is determined, compensation and gain can be added to the amplifier stage to give the desired characteristics: high dc gain, large bandwidth, and a gain with 20dB/decade slope at 0 dB crossover. Because of the slope of closed loop gain at 0dB crossover is 20dB/decade, no compensation is needed.

## III. COMPUTER SIMULATION

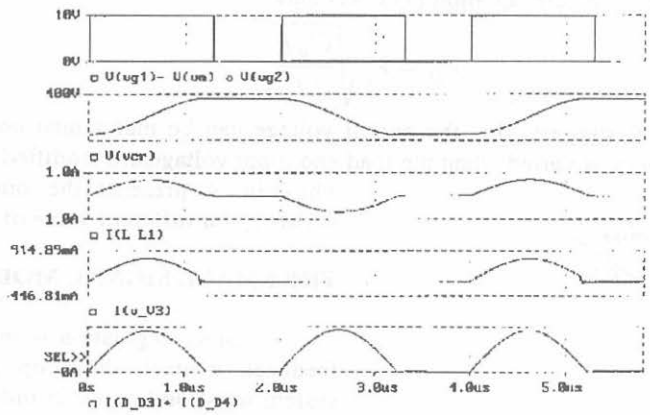


Fig. 5 *The simulated waveforms*

To properly analyze the circuit, simulations have been performed. The Fig. 5 presents SPICE simulation waveforms for mode II. A detail of these waveforms are shown in Fig. 6.

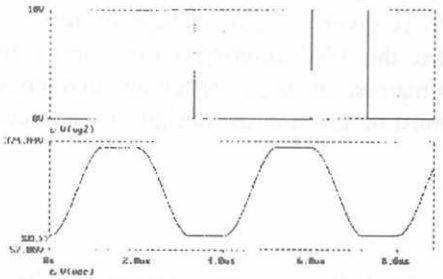

Fig. 6 *A detail for $V_{GS2}$ and $V_{CR}$ voltage.*

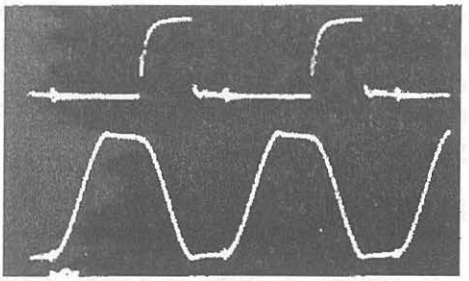

Fig.7 *Upper trace:$V_{GS2}$voltage, V:5V/div; lower trace:$V_{C1}$ :V:100V/div; H:1μs/div*

## IV. PRACTICAL RESULTS

Experimental results for a maximum 400kHz, 60W power converter are presented. The IC circuit used to control the SLCCV is UC 3865 from Unitrode [3,4] and the POWERMOSFETs are driven with the IC IR 2110 from International Rectifier.The input voltage is 350V provided from a power factor correction preregulator [2]. The circuit's scheme is presented in Fig. 8 and the experimental waveforms are presented in Fig 7. As shown in Fig. 6 and Fig. 7 simulated and experimental results agree quite well.

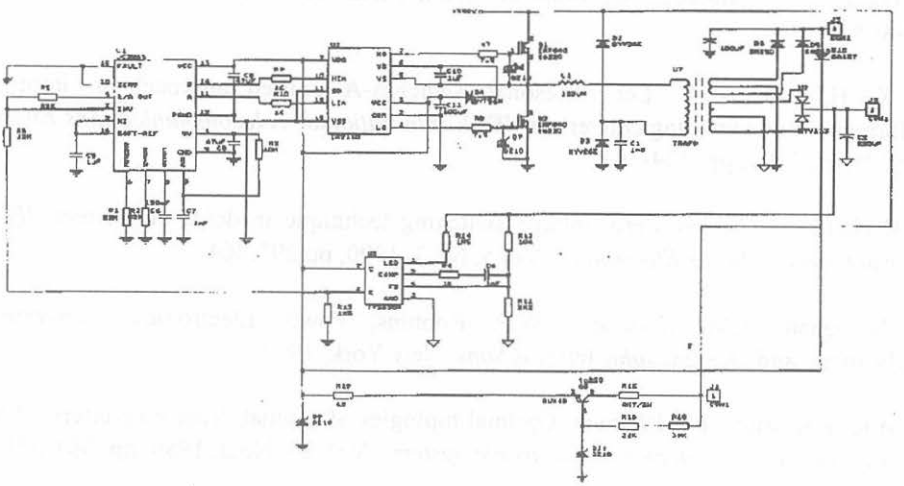

Fig.8 *A SMPS built around SLCCV .*

## V. CONCLUSIONS

A steady-state analysis of the SLCCV has been presented with simulated and experimental waveforms. A small signal analysis for the control loop has also been given. Finally, a complete scheme of SMPS is given. The advantage of resonant converter over the conventional PWM is that the EMI filtering requirements are reduced and efficient operation can be maintained at high switching frequency. However, the drawback exists that more care must be given to the design of the circuit layout and magnetic circuit.

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