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UNIFIED POWER QUALITY CONDITIONER BASED ON CURRENT SOURCE CONVERTER TOPOLOGY

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Abstract: *Nonlinear devices, such as power electronics converters, inject harmonic currents in the AC system and increase overall reactive power demanded by the equivalent load. Also, the number of sensitive loads that require ideal sinusoidal supply voltages for their proper operation has increased. In order to keep power quality under limits proposed by standards, it is necessary to include some sort of compensation. Different types of power quality compensators of higher or lower complexity have been reported. The aim of this paper is to present a unified power quality conditioner (UPQC) that consists of two three-phase current-source converters connected on the same inductive DC link. Such system has faster phase voltage control loop than its voltage-source converter based counterpart, as well as the inherent short circuit protection capability. Also, in this case passive filter connection between UPQC and the load is not needed, which minimizes the cost of the system.*

Keywords*: Active filters, Converter control, Power quality, Harmonics***

1. INTRODUCTION

Nonlinear devices, like power electronics converters, inject harmonic currents in the AC system and increase overall reactive power demanded by the equivalent load. Also, the number of sensitive loads that require ideal sinusoidal supply voltages for their proper operation has increased. In order to keep power quality under limits proposed by standards, it is necessary to include some sort of compensation [1]. During last years a solution based on flexible AC transmission systems (FACTS) have appeared [2]. FACTS converters have been modified to serve in distribution network and, through a modification of a unified power flow controller (UPFC) the unified power quality conditioner (UPQC) [3] was presented during 1998. Such solution can compensate for different power quality phenomena, such as: sags, swells, voltage imbalance, flicker, harmonics and reactive currents.

UPQC usually consists of two voltage-source converters sharing the same capacitive DC link. One of the converters is an active rectifier (AR) while other is a series filter (SF) with a LC ripple filter and transformer isolation from power supply network. Also, at the point of the load connection, passive filter banks are connected.

Voltage-source topology of UPQC has its drawbacks, mainly inside the SF, such as a rather slow control of converters (LC filter) output voltage and current protection problems. Also, when the active rectifier inside UPQC is used as a power factor corrector, DC bus voltage oscillations appear which make the control of the series filter output voltage more difficult. Such problems can be overcome using the current-source converters. The aim of this paper is to present a unified power quality conditioner which consists of two three-phase current-source converters connected on the same inductive DC link, as presented in fig. 1. In this system, AR performs both the DC link current control and the active filtering of the load currents, while SF compensates for the supply voltage imperfections. Such system has faster phase voltage control loop than its voltage-source counterpart, as well as the inherent short circuit protection capability. Also, in this case passive filter connection between UPQC and the load is not necessary, which minimizes the cost of the system.

2. CONVERTER CONFIGURATION

UPQC consists of the:

- Series filter (SF) that compensates supply voltage harmonics, flicker, voltage sags/swells and supply voltage unbalance. Its control equation is:

$$U_{sf} = U_{comp} \tag{1}$$

  where Ucomp is compensation voltage needed to remove supply voltage imperfections. It consists of two components – one extracted by dq theory for harmonics detection, and another determined by the Fortescue transform, for unbalance compensation.
- Active rectifier (AR) for real power transfer to/from common DC bus and for DC bus current control with a unity power factor, as well as shunt harmonic filtering and/or reactive power compensation. DC bus current is maintained constant using three-phase buck converter, controlled in such a way that it is

insensistive to supply voltage imperfections. Control equation of the active rectifier is:

$$I_{ar} = I_{ar1} + I_{pf} \tag{2}$$

where Iar1 is the first harmonic current at the rectifier input, commanded by the DC current control loop and Ipf is the current component for harmonic filtering and power factor correction.

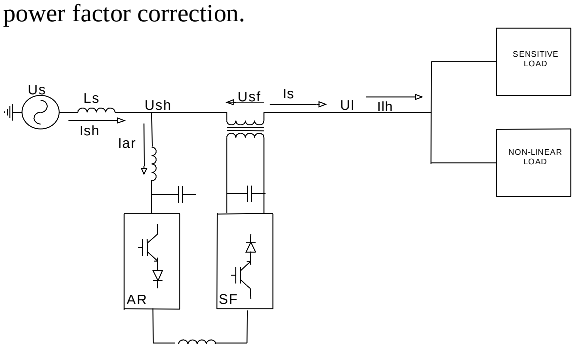

Fig. 1: *UPQC topology using three-phase current-source converters*

3. DERIVATION OF REFERENCE SIGNALS

Control schemes for both parallel and series active filtering usually use the instantaneous reactive power theory (pq theory) [4] for reference signals determination. Although this theory presents a very powerful tool, its implementation is quite involving, since it requires a large number of analog multipliers, dividers, filters etc. Development in DSP technology, its mathematical speed together with fast A/D conversion and different dedicated hardware (space vector modulators, fast digital PWM signal generators) enables the minimization of control hardware and thus the use of the synchronously rotating frame (dq) reference signal derivation [5]. DQ domain quantities of any voltage and current shown in fig. 1 are given by following equations:

$$\begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} = \sqrt{\frac{2}{3}}T \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \text{ and } \begin{bmatrix} u_0 \\ u_d \\ u_q \end{bmatrix} = \sqrt{\frac{2}{3}}T \cdot \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{3}$$

Transformation matrix T, and its inverse are:

$$T = \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ \cos J & \cos\left(J - 2p/3\right) & \cos\left(J - 4p/3\right) \\ -\sin J & -\sin\left(J - 2p/3\right) & -\sin\left(J - 4p/3\right) \end{bmatrix} = T^{-1^{transp.}}$$

$$\text{and} \qquad J = J_0 + \int_0^t w t dt \tag{4}$$

where θ is the instantaneous supply voltage angle, derived from the synchronization circuitry. Currents in rotating frame (either I_{lh}, I_{sh} etc.) can be decomposed in DC (50Hz) and AC (harmonic, sub harmonic or interharmonic) component:

$$i_d = \bar{i}_d + \tilde{i}_d \qquad \text{and} \qquad i_q = \bar{i}_q + \tilde{i}_q \tag{5}$$

where i_d corresponds to the reactive and i_q to the active power component. AC and DC components can be extracted by the means of filtering:

$$\tilde{i}_d(z) = HPF(z) i_d(z) \text{ and } \tilde{i}_q(z) = HPF(z) i_q(z) \tag{6}$$

$$\bar{i}_d(z) = i_d(z) - \tilde{i}_d(z) \text{ and } \bar{i}_q(z) = i_q(z) - \tilde{i}_q(z) \tag{7}$$

One of advantages of a dq domain derivation of reference signals also lies in easier signal filtration, since the 50Hz components are transferred into DC quantities and all harmonic components are AC quantities and therefore no bandpass filtering is necessary. So, HPF(z) is a high-pass digital filter transfer function which can be obtained by the digitalization of its well known first-order analog counterpart HPF(s):

$$HPF(z) = HPF(s)\Big|_{s=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}} = \frac{s}{s+w_c}\Bigg|_{s=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}} = \frac{2\left(1-z^{-1}\right)}{\left(2+w_c T\right) - \left(2 - w_c T\right)z^{-1}} \tag{8}$$

where T is the sampling period. Sampling period for proper filtering has to be at least $T<T_h/4$, where T_h is the period of the highest harmonic component to be eliminated ($T_h=1/f_h$). For instance if a highest harmonic is 21. then T should approximately be 1ms. Based on these consideration, reference currents for parallel filtering task of AR can be calculated as in left part of (9) if only harmonics are to be eliminated, or as in right part of (9) if power factor has to be corrected together with the harmonic elimination:

$$\begin{bmatrix} i^*_{pfa} \\ i^*_{pfb} \\ i^*_{pfc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos J & -\sin J \\ \cos\left(J - 2p/3\right) & -\sin\left(J - 2p/3\right) \\ \cos\left(J - 4p/3\right) & -\sin\left(J - 4p/3\right) \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_{lhd} \\ \tilde{i}_{lhq} \end{bmatrix}$$

$$\begin{bmatrix} i^*_{pfa} \\ i^*_{pfb} \\ i^*_{pfc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos J & -\sin J \\ \cos\left(J - 2p/3\right) & -\sin\left(J - 2p/3\right) \\ \cos\left(J - 4p/3\right) & -\sin\left(J - 4p/3\right) \end{bmatrix} \cdot \begin{bmatrix} \bar{i}_{lhd} + \tilde{i}_{lhd} \\ \tilde{i}_{lhq} \end{bmatrix} \tag{9}$$

Reference voltages for the series active filter can be determined based on same procedure, starting from (1). Again, if only harmonic compensation is required, reference voltages are as in left part of (10), but if the voltage compensation is required, then reference voltages are as in right part of (10):

$$\begin{bmatrix} u^*_{sfa} \\ u^*_{sfb} \\ u^*_{sfc} \end{bmatrix} = K\sqrt{\frac{2}{3}}T^{-1} \cdot \begin{bmatrix} \tilde{i}_{shd} \\ \tilde{i}_{shq} \\ i_0 \end{bmatrix}$$

$$\begin{bmatrix} u^*_{sfa} \\ u^*_{sfb} \\ u^*_{sfc} \end{bmatrix} = K\sqrt{\frac{2}{3}}T^{-1} \cdot \begin{bmatrix} \tilde{i}_{shd} \\ \tilde{i}_{shq} \\ i_0 \end{bmatrix} + \begin{bmatrix} u_{compa} \\ u_{compb} \\ u_{compc} \end{bmatrix} \tag{10}$$

where voltage compensation factor is as in (11):

$$\begin{bmatrix} u_{compa} \\ u_{compb} \\ u_{compc} \end{bmatrix} = \sqrt{\frac{2}{3}}T^{-1} \cdot \begin{bmatrix} u_{compd} \\ u_{compq} \\ u_{comp0} \end{bmatrix} \qquad \text{where}$$

$$\begin{bmatrix} u_{compd}(s) \\ u_{compq}(s) \\ u_{comp0}(s) \end{bmatrix} = \begin{bmatrix} \left(u_{dnom}(s) - u_d(s)\right) \\ \left(u_{qnom}(s) - u_q(s)\right) \\ \left(u_{0nom}(s) - u_0(s)\right) \end{bmatrix} \tag{11}$$

Nominal d, q, and zero voltage are precalculated from the ideal voltage supply waveform and are equal to: $U_{dnom}=0$, $U_{0nom}=0$ and $U_{qnom}=380$.

4. CONTROL OF CURRENT SOURCE CONVERTERS

Control structure for current source converter based UPQC is presented in fig. 2. Voltage reference signals, as derived in preceeding section, are compared to actual output voltages. Their diference (voltage error) is fed to hysteresis comparators forming the inverter bi-level switching signals SB_{SF}. Rectified and filtered voltage error forms DC bus current reference (Id*). DC bus current is controlled by simple PI controler, which output is synchronised with individual supply phase voltages, forming the first harmonic current reference component - Iar1* as in (2). These components are added to the active filtering references given in (9), forming the final AR phase current references. These references are compared to the actual currents at the converters input and their difference is fed to the hysteresis controller which output is then AR bi-level switching signals SB_{AR}.

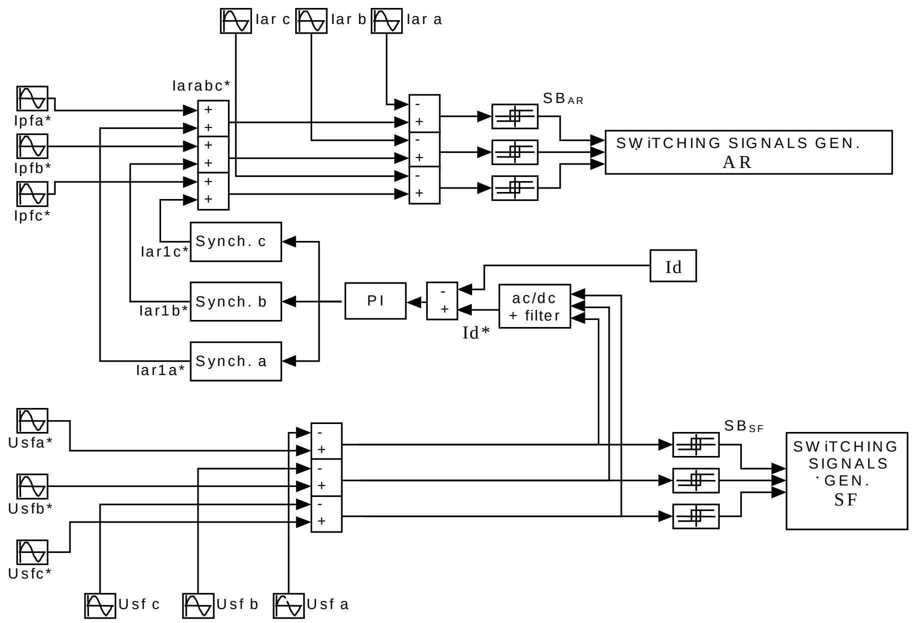

Fig. 2: *UPQC Control structure*

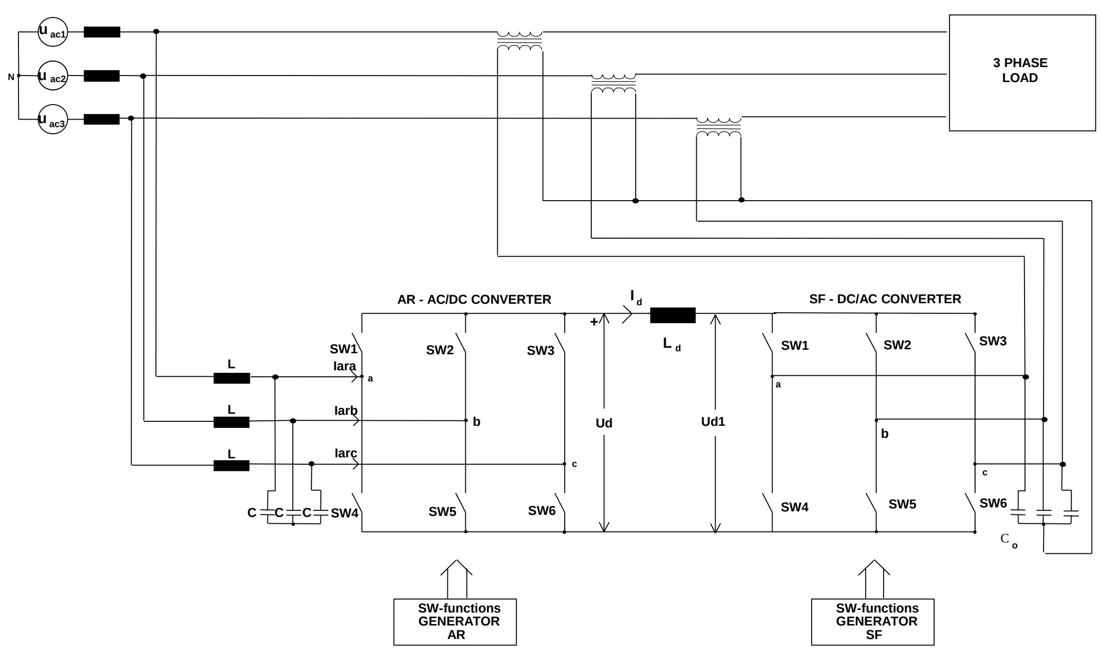

Fig. 3: *Converter structure with switching functions generators*

Fig. 3 shows converter structure with switching functions generators. Since derivation of the transistor gating signals from bi-lateral switching signal is the same for both AC/DC and DC/AC converter index (AR or SF) will be omitted.

As mentioned before, output of the hysteresis controller yields bi-level switching signals for converter legs A, B and C, necessary for the converter control. Formation of the final transistor switching signals is based on the following procedure [6]: from the bi-level signal (SB_i, i=A,B,C), a tri-level leg switching function signal (ST_i, i=A,B,C), necessary for proper operation of the converter, is derived:

$$ST_A = SB_A - SB_B \;;\; ST_B = SB_B - SB_C \;; \quad ST_C = SB_C - SB_A \tag{12}$$

Then the bi-level switching functions of the transistors are:

$$ST1=\begin{cases}1 & ST_A>0\\0 & ST_A\le 0\end{cases}\quad ST2=\begin{cases}1 & ST_B<0\\0 & ST_B\ge 0\end{cases}\quad ST3=\begin{cases}1 & ST_C<0\\0 & ST_C\ge 0\end{cases}$$
$$ST4=\begin{cases}1 & ST_A<0\\0 & ST_A\ge 0\end{cases}\quad ST5=\begin{cases}1 & ST_B<0\\0 & ST_B\ge 0\end{cases}\quad ST6=\begin{cases}1 & ST_C<0\\0 & ST_C\ge 0\end{cases} \tag{13}$$

For the inductive type loads, it is necessary to ensure the existence of the DC current path. It can be done in two ways. If the regenerative (inverter) mode of operation is not required, a freewheeling diode can be used. In that case, the bi-level transistor switching signals correspond to final gating signals of the converter switches SWi=STi, i=1,..,6. This approach also minimizes the conduction losses of the active power switches. If the inverter mode of operation is necessary, the alternative current path for the DC current must be obtained within the converter. Since only two of the switches are conducting at the same time (one in the upper and one in the lower part of the bridge), the gating signals can be derived from the bi-level transistor switching functions (STi, i=1,..,6) in the following manner:

$$\begin{aligned}
SW1 &= ST1 \vee (\overline{ST1} \wedge \overline{ST2} \wedge \overline{ST3} \wedge ST4)\\
SW2 &= ST2 \vee (\overline{ST1} \wedge \overline{ST2} \wedge \overline{ST3} \wedge ST5)\\
SW3 &= ST3 \vee (\overline{ST1} \wedge \overline{ST2} \wedge \overline{ST3} \wedge ST6)\\
SW4 &= ST4 \vee (\overline{ST4} \wedge \overline{ST5} \wedge \overline{ST6} \wedge ST1)\\
SW5 &= ST5 \vee (\overline{ST4} \wedge \overline{ST5} \wedge \overline{ST6} \wedge ST2)\\
SW6 &= ST6 \vee (\overline{ST4} \wedge \overline{ST4} \wedge \overline{ST6} \wedge ST3)
\end{aligned} \tag{14}$$

This means that the switch SWi should be gated either when its tri-level function is active or when the complementary transistor is conductive, but none of the switches in the same part of the bridge (upper or lower) have active tri-level function.

It has been shown in [7] that stability requirements in case of the linear current control of the AC/DC converter demand introduction of a damping resistor of significant value into an AC filter. Therefore, in this paper the hysteresis current controller has been chosen to improve the overall efficiency of the system. In such a case, it is important to derive the maximum switching frequency f_{sw}. Since a current source converter, fed from the LC filtered voltage source, represents the second order system, only an implicit expression can be derived. It gives correlation between filter (L and C) components, hysteresis band (H_{AR}) and the switching frequency [6]:

$$H_{AR} = \frac{U_{ac}}{4Lf_{swAR}} - \frac{H_{AR}}{24LCf_{swAR}^{2}} + \frac{I_d}{16LCf_{swAR}^{2}} \tag{15}$$

Such dependence can lead to very high switching frequencies in certain extreme conditions. In order to prevent appearance of too high switching frequencies, a clocked hysteresis controller is used, limiting the switching frequency to f_{sw}=20kHz. In the case of capacitive loaded current source DC/AC conversion, the maximum inverters switching frequency is more straightforward:

$$f_{swSF} = \frac{I_d}{4H_{SF}C_o} \tag{16}$$

5. SIMULATION RESULTS

Complete system (converters, control circuitry, supply, load) has been simulated using SIMULINK toolbox from MATLAB 4.2. The UPQC and its control system have been tested at different load/supply imperfections. Fig. 4 shows series filter output voltage in the case of 20 % voltage sag. It can be seen that SF phase voltage accurately tracks the reference. Figures 5 and 6 are displaying AR behavior, showing sinusoidal input currents in phase with supply voltages, with fast reference tracking capability. Step change in commanded current is rapidly obtained, without oscillations typical for the PWM control of active current-source converters. AR operation as a parallel filter compensating a 30 kW DC motor drive is presented in figures 7 and 8. Figures 9. and 10. show UPQC operation in the case of polluted supply voltage, having the 5th and 7th harmonic at levels of 10% and 7% respectively. SF output voltage and DC link current for the same case are presented in fig. 11. and fig. 12.

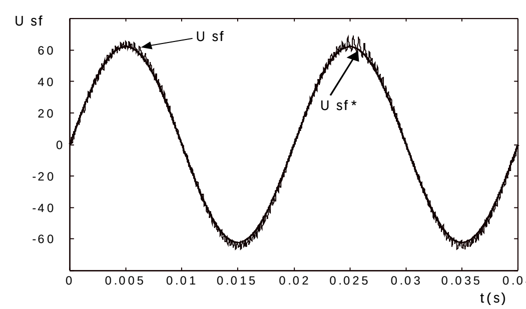

Fig.4: *Series filter output voltage in the case of 20 % voltage sag*

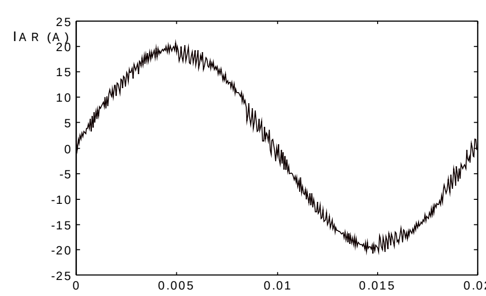

Fig. 5: *On-line control of active rectifier - typical period of AR line current*

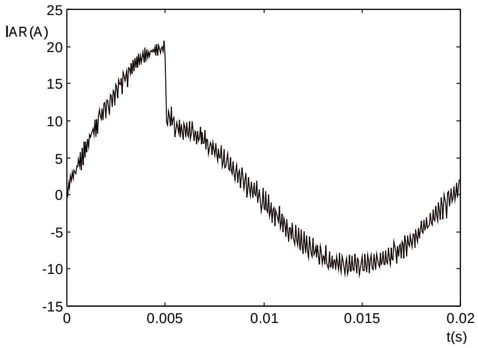

Fig. 6: *AR line current response on the step change in commanded DC current*

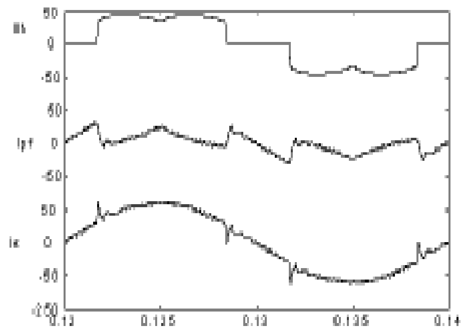

Fig. 7: AR operation as a harmonics filter -Load, AR and line current

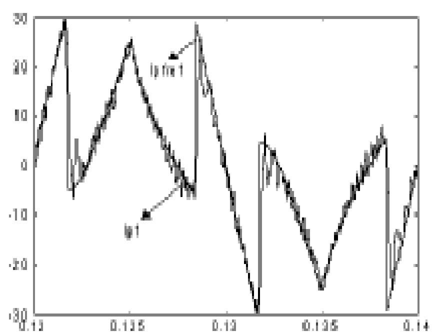

Fig. 8: *AR operation as a harmonic filter -reference and actual AR current*

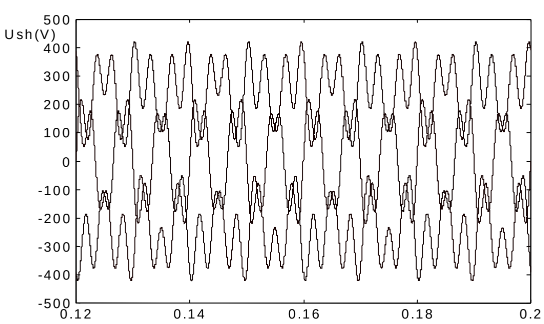

Fig. 9: *Poluted supply voltage - 5^{th} and 7^{th} harmonic at levels of 10% and 7%*

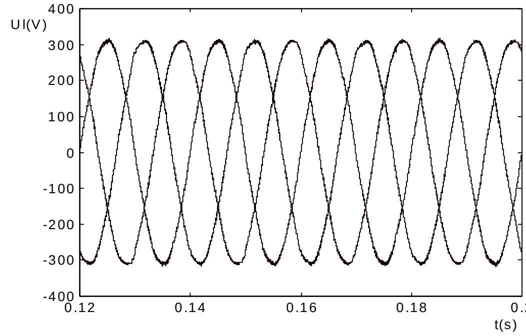

Fig. 10: *Load voltage - 5^{th} and 7^{th} harmonic at levels of 10% and 7% in supply voltage*

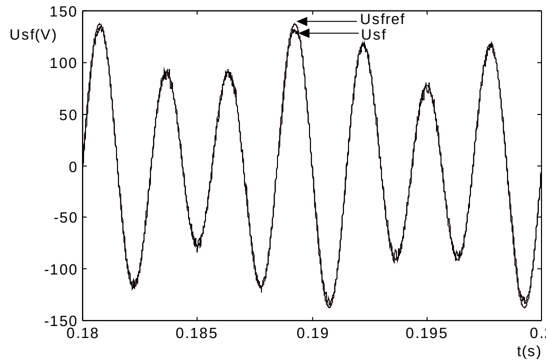

Fig. 11: *SF voltage - 5^{th} and 7^{th} harmonic at levels of 10% and 7% in supply voltage*

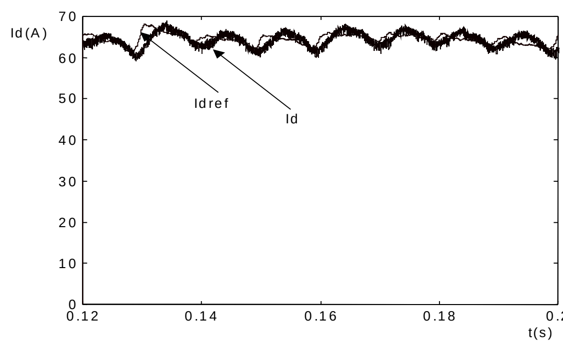

Fig. 12: DC bus current – 5^{th} and 7^{th} harmonic at levels of 10% and 7% in supply voltage

Tracking error appearing in the DC bus current was introduced from the stability reasons, but it does not influence the SF output voltage performance. Oscilations of DC current around its medium value are caused by compensation of nonsinusoidal voltages. Similar DC current waveshape appears also when AR compensates for load power factor, but, as in previous case, it does influence the performance of the system. Figures 13. – 15. show UPQC transient responce at 30% undervoltage in the supply.

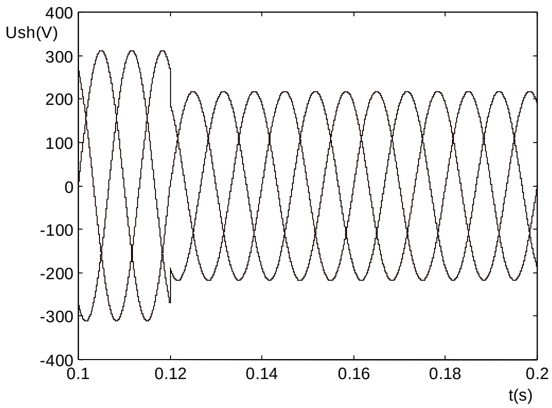

Fig. 13: *Supply voltage - 30% undervoltage*

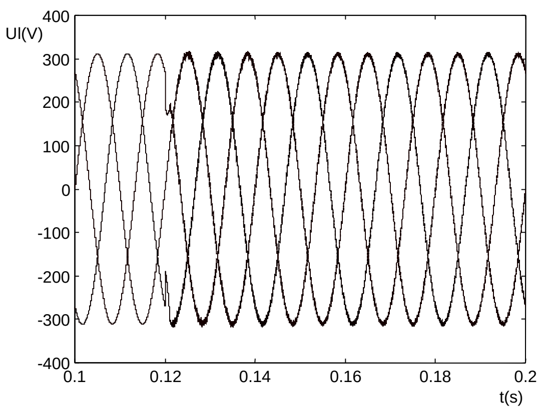

Fig. 14: *Load voltage - 30% supply undervoltage*

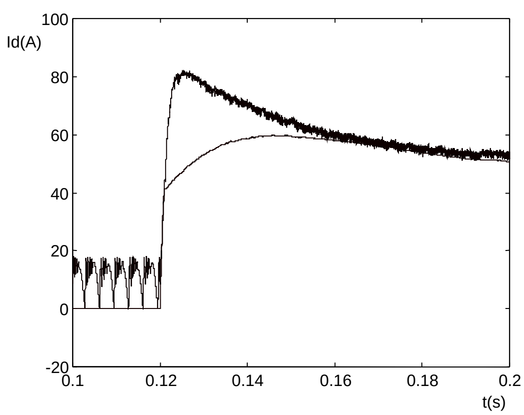

Fig. 15: *DC bus current - 30% supply undervoltage*

6. CONCLUSION

In this paper a unified power quality conditioner based on current source converter topology was presented. It consists of two three-phase current-source converters of one of which is a current-source rectifier and another is a current-source inverter. Control structure, together with converter gating generation were presented. Advantages of this system are:

- Faster phase voltage controll loop than its voltage-source converter based counterpart
- No passive filter between converter and load
- Inherent short circuit protection capability as with all current source converters

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