Paper No. T1-2.8, pp. 1-5

11th INTERNATIONAL SYMPOSIUM on
POWER ELECTRONICS - Ee 2001
XI Međunarodni simpozijum Energetska elektronika – Ee 2001
NOVI SAD, YUGOSLAVIA, OCT. 31 – NOV. 2, 2001

MULTISTEP INDUCTORLESS DC-DC TRANSFORMER WITH HIGH VOLTAGE RATIO

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Abstract: *The four-stage (five-step) high-voltage-ratio inductorless DC-to-DC converter is analyzed. Geometric progression capacitance-ratio is proposed. Significant improvement of the output resistance is obtained. A prototype is constructed with capacitance ratio of two and output power of approximately 300W. Its characteristics are examined by simulations and measurement.*

Key Words: ***Power Converter, Inductorless***

1. INTRODUCTION

Inductorless power converters are subjects of intensive research activities recently. They are mainly low-power high-frequency converters (several watts to several tens of watts) intended for hybridization.

The earliest known inductorless converter is the Cockcroft-Walton voltage multiplier [1]. This simple circuit provides low-power high voltage but at an expense of double the number of capacitors for the voltage ratio than the classical converter. Classical converters have output-to-input voltage ratios equal to the number of capacitors [2] or voltage ratios that grow by the Fibonacci series [3] with the number of capacitors. All previous converters operate in two steps i.e. have two functional states in which charge is transferred.

A special type of transformers are the high-voltage-ratio transformers [4] that operate in more than two steps. Their voltage ratio grows at a geometric progression with the number of capacitors. They have been well investigated in the case when the components (capacitors and switches) can be assumed as ideal, but with all the capacitors equal. If it seams reasonable for the classical converters, since the voltage of the capacitors are equal, a geometric ratio of the capacitors in the later ones may be expected to give better performances. This article proves the previous assumption by analytical means, simulations and prototype measurements on a four stage converter from 42V (emerging car-battery voltage) to 620V (needed for PWM generation of AC-line voltage) at 0.5A .

2. PRINCIPLE OF OPERATION

The circuit is shown in Fig. 1 and the timing diagrams of the switches are shown in Fig. 2.

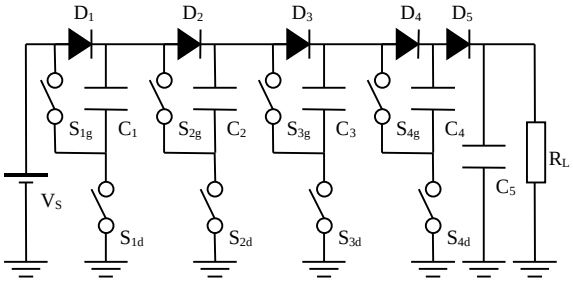

Fig. 1. *Circuit diagram*

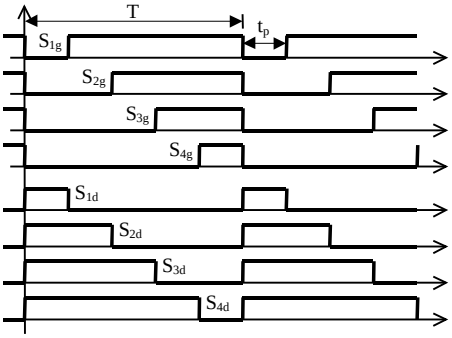

Fig. 2. *Timing diagrams*

There are four steps (one more than the number of capacitors) in one cycle. This is illustrated in Fig. 3. It also shows the voltages of the capacitors at no load. Each of the capacitors is charged during one of the steps consecutively, and discharged during the following steps. The ideal voltage ratio is 2^n where n is the number of stages (switched capacitors). The last capacitor is actually the filter capacitor that supplies the load during the first n (four) steps and charges during the last (n+1)-th (fifth) step.

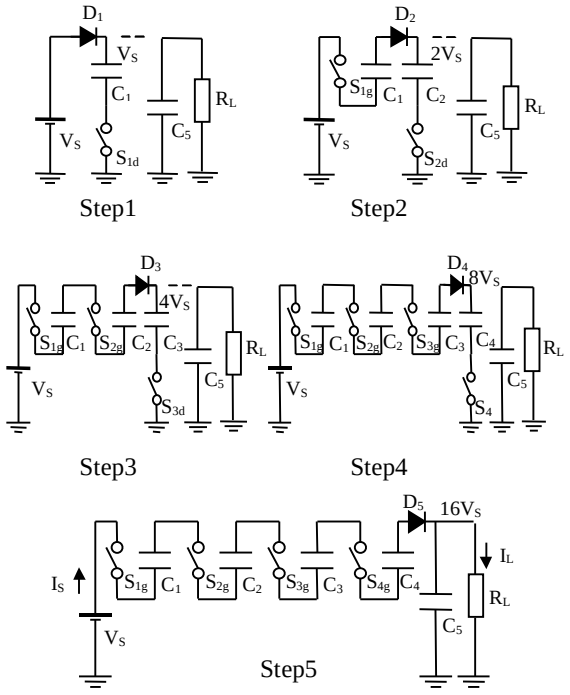

Fig. 3. *Circuit operation steps*

3. CONVERTER ANALYSIS

It has been shown in [4] that in the case of ideal components the output-to-input average-current ratio is independent on capacitor values and depends only on circuit configuration:

$$\bar{I}_L = \frac{\bar{I}_S}{2^n}, \tag{1}$$

where $\bar{I}_L$ is the average load current and $\bar{I}_S$ is the average current through the source V_S. For the four-stage converter we obtain $\bar{I}_L = \bar{I}_S / 2^4$.

For derivation of the output voltage expression the capacitances of the capacitors are needed. The assumption for geometric distribution of the capacitances among converter stages can be expressed with the following relationships:

$$C_5 = C; C_4 = kC; C_3 = k^2 C; C_2 = k^3 C; C_1 = k^4 C. \tag{2}$$

The output voltage (as shown in the Appendix) can be expressed with the following equation:

$$\bar{V}_L \approx V_{Lm} - \bar{I}_L \cdot R_O, \tag{3}$$

where V_{Lm} is the no-load output voltage

$$V_{Lm} = 2^4 \cdot V_S, \tag{4}$$

and R_O is the so-called switched-capacitor resistance:

$$R_O = \frac{1}{fC} \frac{43+11k+3k^2+k^3}{k^4}. \tag{5}$$

Here $f = 1/T$ is the switching frequency and $R_0 = 1/fC$ is the "basic" switched-capacitor resistance.

The DC-output efficiency expression follows directly from the previous equations:

$$h = \frac{\bar{V}_L \bar{I}_L}{V_S \bar{I}_S} = \frac{\bar{V}_L}{2^4 V_S} = 1 - \frac{\bar{I}_L R_O}{2^4 V_S}. \tag{6}$$

It is obvious that lowering the output resistance R_O can increase the efficiency of the converter. This imposes the dependence of the efficiency on parameter *k*. There are two cases in practice: discrete component converter and on-chip converter.

With discrete component converter a general rule is applicable: higher value capacitors are available at lower voltage ratings. This is in perfect agreement with the reverse voltage-rating dependence of the capacitors in this converter compared with the capacitance dependence. The normalized output resistance dependence on the parameter *k* (i.e. compared with the resistance at *k*=1) is shown in Fig. 4.

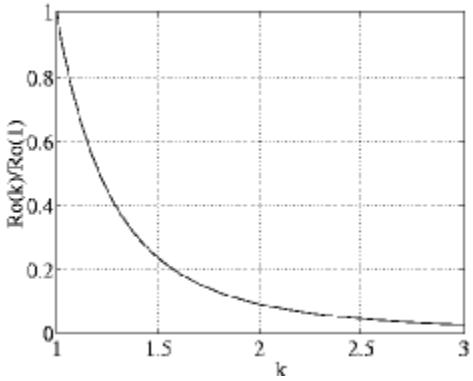

Fig. 4. *Normalized output resistance for discrete component converter*

A steep reduction of the output resistance can be noticed up to values of 1.5 to 2 for the parameter *k*, after which the curve becomes nearly flat.

For the on-chip converters the most important is the total area that is occupied by the converter which actually means the total capacitance:

$$C_{tot} = C_1 + C_2 + C_3 + C_4 + C_5. \tag{7}$$

In this case the output resistance expression becomes:

$$R_O = \frac{1}{fC_{tot}} \frac{\left(43+11k+3k^2+k^3\right)\left(k^4+k^3+k^2+k+1\right)}{k^4}. \tag{8}$$

The graphical representation of the normalized resistance dependence on the parameter *k* is presented in Fig. 5.

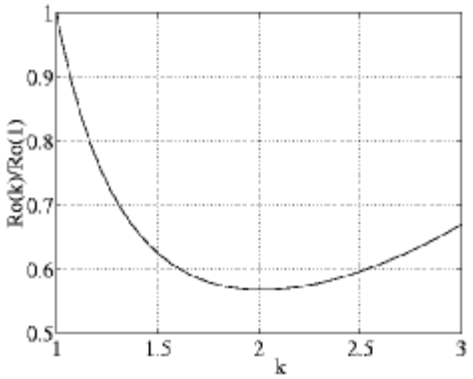

Fig. 4. *Normalized output resistance for the on-chip converter*

A minimum at k=2 can be noticed where the output resistance reduction is nearly 45% with the same total chip-area occupied.

Another important issue is the output voltage ripple. A conservative result is obtained by assuming that C_5 is supplying the load alone:

$$V_{Lr} \approx \frac{I_L T}{C_5} = \frac{I_L}{fC}. \quad (9)$$

4. EXPERIMENTAL RESULTS

A prototype has been constructed with discrete components (Table 1).

Table 1. *Prototype components*

Stage:	1	2	3	4	5
Capacitance µF	2200	800	440	220	110
Voltage V	63	400	250	400	800
Measured ESR mΩ	40	120	70	120	240
Switch	IRFZ 44	IRF5 4052	IRF6 40	IRF8 4085	
RDSon mΩ	22		180	0	
Photocouplers	Sharp PC 847 (⇔ 4x4N36)				

The idea is to obtain a voltage of about 600V from the 42V (emerging) car-battery voltage at power level (approx. 300W i.e. I_L≈0.5A) that is an order of magnitude higher than the usual for discrete inductorless converters. At this power level, limitations appear for the RMS current through the capacitors (especially C_1). The absolute average value of it's current is 8A and the form-factor (see Appendix) is al least 1.3 which means RMS current of 10.4A. If highest quality electrolytic capacitors are used than their capacitance (at 50–63V voltage rating) should be at least 5600µF [5]. At capacitance ratio of k=2, the output capacitance should be C_5=350µF with voltage rating higher than 700V and, consequently, the frequency for 1% output voltage ripple would be

$$f \approx \frac{I_L}{V_{Lr} C} = \frac{0.5}{6 \cdot 0.35 \cdot 10^{-3}} = 240 Hz. \quad (10)$$

Since electrolytic capacitors have best performances at frequencies of 1-5kHz, as a compromise a frequency of 2kHz has been chosen with the values of the components from Table 1 and intermittent operation of the converter. This allows the use of ordinary photocouplers for the driving circuitry.

The dependence of the characteristics on various parameters of the converter has been investigated by PSpice simulation and is presented in Fig. 5 through Fig 7. The measured characteristics of the prototype are shown in Fig. 8.

It is interesting to note that all the simulation diagrams show extremely high overlapping of the efficiency and normalized output voltage curves. This means that the equation (6), derived for the idealized converter, is also valid for the non-idealized converter. The difference that appears in the measured characteristics is because of the power for the switch-driving circuitry that was taken from the input voltage source.

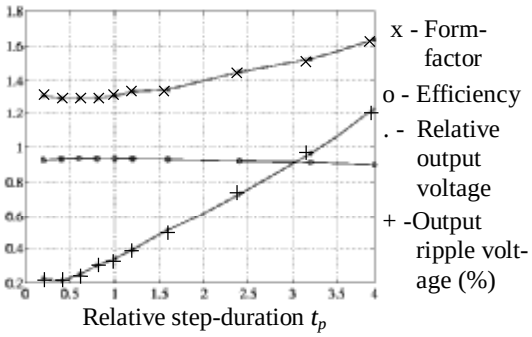

Fig. 5. *Simulated converter characteristics dependence on step duration*

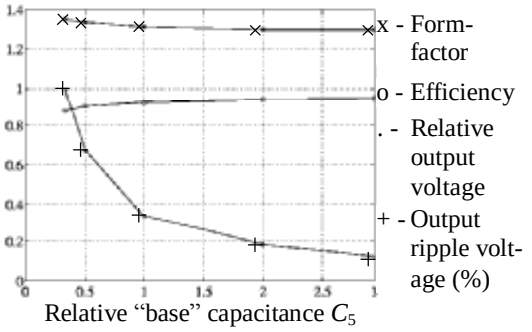

Fig. 6. *Simulated converter characteristics dependence on »base« capacitance C*

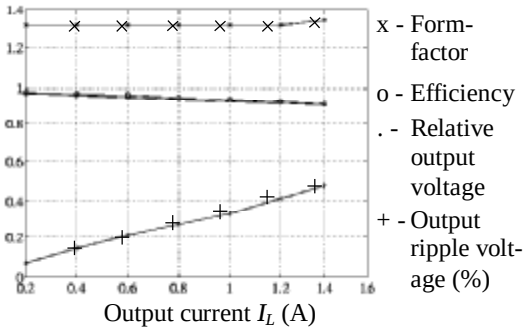

Fig. 7. *Simulated converter characteristics dependence on output current I_L*

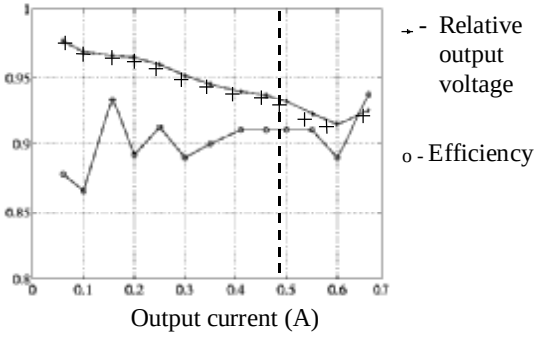

Fig. 8. *Measured converter characteristics*

5. CONCLUSIONS

The non-uniform distribution of the capacitance in the multistep inductorless DC-to-DC converter with high voltage ratio in a form of geometric series, results in significant improvements of the converter characteristics. This is derived analytically for the idealized converter and shown by simulation for the real converter.

Prototype measurement results show high stability of the output within wide load variations and more than 90% efficiency.

6. REFERENCES

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[5] Cornell-Dubilier: Aluminum Electrolytic Capacitors; www.cornell-dubilier.com

7. APPENDIX

Following the methodology in [4] we can write: Let $\Delta Q_{Ci}^{(j)}$ denote the charge transferred into capacitor C_i during the step j. The charge into the load during one cycle is:

$$\Delta Q_L = \bar{I}_L \cdot T \,. \tag{A1}$$

In steady state total charge transfer into each capacitor is zero and each capacitor is charged only once – at the beginning of the corresponding step. The charge transferred through the switched-capacitors (1 through 4) during the fifth step is the total charge delivered to the load. From this follow the equations:

$$\Delta Q_{C1}^{(5)} = \Delta Q_{C2}^{(5)} = \Delta Q_{C3}^{(5)} = \Delta Q_{C4}^{(5)} = -\Delta Q_L \tag{A2}$$

$$\Delta Q_{C4}^{(4)} = -\Delta Q_{C4}^{(5)} = \Delta Q_L \tag{A3}$$

$$\Delta Q_{C1}^{(4)} = \Delta Q_{C2}^{(4)} = \Delta Q_{C3}^{(4)} = -\Delta Q_{C4}^{(4)} = -\Delta Q_L \tag{A4}$$

$$\Delta Q_{C3}^{(3)} = -\Delta Q_{C3}^{(4)} - \Delta Q_{C3}^{(5)} = 2\Delta Q_L \tag{A5}$$

$$\Delta Q_{C1}^{(3)} = \Delta Q_{C2}^{(3)} = -\Delta Q_{C3}^{(3)} = -2\Delta Q_L \tag{A6}$$

$$\Delta Q_{C2}^{(2)} = -\Delta Q_{C2}^{(3)} - \Delta Q_{C2}^{(4)} - \Delta Q_{C2}^{(5)} = 4\Delta Q_L \tag{A7}$$

$$\Delta Q_{C1}^{(2)} = -\Delta Q_{C2}^{(2)} = -4\Delta Q_L \tag{A8}$$

$$\Delta Q_{C1}^{(1)} = -\Delta Q_{C1}^{(2)} - \Delta Q_{C1}^{(3)} - \Delta Q_{C1}^{(4)} - \Delta Q_{C1}^{(5)} = 8\Delta Q_L \tag{A9}$$

The total charge from the source is:

$$\Delta Q_S = \Delta Q_{C1}^{(1)} - \Delta Q_{C1}^{(2)} - \Delta Q_{C1}^{(3)} - \Delta Q_{C1}^{(4)} - \Delta Q_{C1}^{(5)} = 16\Delta Q_L \tag{A10}$$

From (A1) and (A10) we obtain:

$$\bar{I}_S = \frac{\Delta Q_s}{T} = 2^4 \bar{I}_L \,. \tag{A11}$$

The output voltage expression can be derived by following the voltages of the capacitors at the end of each step $V_{Ci}^{(j)}$:

$$V_{C1}^{(1)} = V_S \tag{A12}$$

$$V_{C1}^{(2)} = V_S - \frac{\Delta Q_{C1}^{(2)}}{C_1} = V_S - \frac{4\Delta Q_L}{k^4 C} \tag{A13}$$

$$V_{C1}^{(3)} = V_{C1}^{(2)} - \frac{\Delta Q_{C1}^{(3)}}{C_1} = V_S - \frac{6\Delta Q_L}{k^4 C} \tag{A14}$$

$$V_{C1}^{(4)} = V_{C1}^{(3)} - \frac{\Delta Q_{C1}^{(4)}}{C_1} = V_S - \frac{7\Delta Q_L}{k^4 C} \tag{A15}$$

$$V_{C1}^{(5)} = V_{C1}^{(4)} - \frac{\Delta Q_{C1}^{(5)}}{C_1} = V_S - \frac{8\Delta Q_L}{k^4 C} \tag{A16}$$

$$V_{C2}^{(2)} = V_S + V_{C1}^{(2)} = 2V_S - \frac{4\Delta Q_L}{k^4 C} \tag{A17}$$

$$V_{C2}^{(3)} = V_{C2}^{(2)} - \frac{\Delta Q_{C2}^{(3)}}{C_2} = 2V_S - \frac{\Delta Q_L}{k^4 C}(4+2k) \tag{A18}$$

$$V_{C2}^{(4)} = V_{C2}^{(3)} - \frac{\Delta Q_{C2}^{(4)}}{C_2} = 2V_S - \frac{\Delta Q_L}{k^4 C}(4+3k) \tag{A19}$$

$$V_{C2}^{(5)} = V_{C2}^{(4)} - \frac{\Delta Q_{C2}^{(5)}}{C_2} = 2V_S - \frac{\Delta Q_L}{k^4 C}(4+4k) \tag{A20}$$

$$V_{C3}^{(3)} = V_S + V_{C1}^{(3)} + V_{C2}^{(3)} = 4V_S - \frac{\Delta Q_L}{k^4 C}(10+2k) \tag{A21}$$

$$V_{C3}^{(4)} = V_{C3}^{(3)} - \frac{\Delta Q_{C3}^{(4)}}{C_3} = 4V_S - \frac{\Delta Q_L}{k^4 C}(10+2k+k^2) \tag{A22}$$

$$V_{C3}^{(5)} = V_{C3}^{(4)} - \frac{\Delta Q_{C3}^{(5)}}{C_3} = 4V_S - \frac{\Delta Q_L}{k^4 C}(10+2k+2k^2) \tag{A23}$$

$$V_{C4}^{(4)} = V_S + V_{C1}^{(4)} + V_{C2}^{(4)} + V_{C3}^{(4)} = 8V_S - \frac{\Delta Q_L}{k^4 C}(21+5k+k^2) \tag{A24}$$

$$V_{C4}^{(5)} = V_{C4}^{(4)} - \frac{\Delta Q_{C4}^{(5)}}{C_4} = 8V_S - \frac{\Delta Q_L}{k^4 C}(21+5k+k^2+k^3) \tag{A25}$$

$$V_L \approx V_{C5}^{(5)} = V_S + V_{C1}^{(5)} + V_{C2}^{(5)} + V_{C3}^{(5)} + V_{C4}^{(5)} = 16V_S - \frac{\Delta Q_L}{k^4 C}(43+11k+3k^2+k^3) \tag{A26}$$

The form factor (FF) of the current through C_1 can be obtained from Fig. A1:

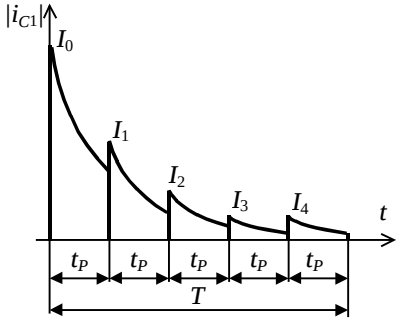

Fig. A1. *Absolute current through* C_1

The average and RMS values of the waveform are:

$$I_{AVG} = \frac{1}{T}\sum_i \int_0^{t_P} I_i e^{-\frac{t}{t}} dt = \frac{t}{T}\left(1 - e^{-\frac{t_P}{t}}\right)\sum_i I_i \qquad \text{(A27)}$$

$$I_{RMS}^2 = \frac{1}{T}\sum_i \int_0^{t_P} I_i^2 e^{-\frac{2t}{t}} dt = \frac{t}{2T}\left(1 - e^{-\frac{2t_P}{t}}\right)\sum_i I_i^2 \qquad \text{(A28)}$$

where $I_1 = I_0 / 2$, $I_2 = I_0/4$ and $I_3 = I_4 = I_0/8$.

The two limiting cases are:

a) $t_P << t$ (nearly "flat" current pulses; partial charge transfer) $\Rightarrow$

$$I_{AVG} \approx \frac{t_P}{T}\sum_i I_i \text{ and } I_{RMS} \approx \sqrt{\frac{t_P}{T}}\sqrt{\sum_i I_i^2} \qquad \text{(A29)}$$

Knowing t_P=T/5 and current relations given above, we obtain:

$$FF_a = \frac{I_{RMS}}{I_{AVG}} \approx 1.296 . \qquad \text{(A30)}$$

b) $t_P >> t$ (Down to "zero" current pulses; complete charge transfer) $\Rightarrow$

$$I_{AVG} \approx \frac{t}{T}\sum_i I_i \text{ and } I_{RMS} \approx \sqrt{\frac{t}{2T}}\sqrt{\sum_i I_i^2} \qquad \text{(A31)}$$

In this case:

$$FF_b = \frac{I_{RMS}}{I_{AVG}} \approx 0.916\sqrt{\frac{t_P}{t}} . \qquad \text{(A32)}$$

The boundary of complete charge transfer is $t_P \approx 3t$, which gives $FF \approx 1.587$.