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EXCESSIVE POWER DISSIPATION IN PWM DRIVE UNITS

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Abstract: *For experimental purposes an AC 3 phase drive unit was built. The system was constructed of two mutually insolated sections in order to facilitate experiments by the students. With the initial experiments excessive power dissipation was noticed in no load conditions, and the cause of the problem was detected and eliminated.*
Key Words: ***3 Phase PWM Drive unit***

1. INTRODUCTION

The system is built around DSC (digital signal controller) 56F8322 product of Freesscale, as a control unit, while a power hybrid drive circuit IRMAX 16UP60 was used for the output section. This unit is produced by IRF.[1]. The intention was to built a system with full galvanic insulation in order to minimize potential risks to the users, especially students that are involved in particular experiments. For the current sensing two hall based sensors were selected, product of LEM, and theirs respective analog voltage outputs were feed to the analog to digital converter of the DSC. For the voltage sensing an insulation amplifier was used. This is maybe not the cheapest approach, but is intuitive one and most clear to the students. The steering pulses from the digital control section are transferred via optocoupler units and are further buffered and feed to the hybrid output unit. The system has also an user interface that consists of a display unit and a set of switches and a single potnentiometer. The system operates from a single phase power supply. The simplified concept of the system is presented on Fg.1

2. DESCRIPTION OF THE PROBLEM

When the system was put to work, an excessive power dissipation was detected, despite the heat sink that was used. Dimensions of the heat sink were according to the recommendations of the producer of the power hybrid module, so the problem was located elsewhere. The initial experiments were performed with light load and that was indication that the source of the problem is within the design or a bed component is inserted. The cause of the problem was note clear at first, so two strategies were established. With the first approach an analytical model of the drive section was evaluated and some calculations for the power dissipation were performed. The system was tested with ideal drive signals[2][3] and the results of the simulation showed that the power dissipation is close to 1[W]. The model that was used for simulation is presented on Fig.2. From the simulation, waveforms of the drive currents and voltages were obtained, and they were very close to the theoretical ones. It was clear that the only possibility for excessive dissipation may arise if only two high/low transistors of the output drive unit are conducting simultaneously. This is due to the fact that the drive stage for the output IGBTs is inside the hybrid unit and the on state is very well defined and achieved.

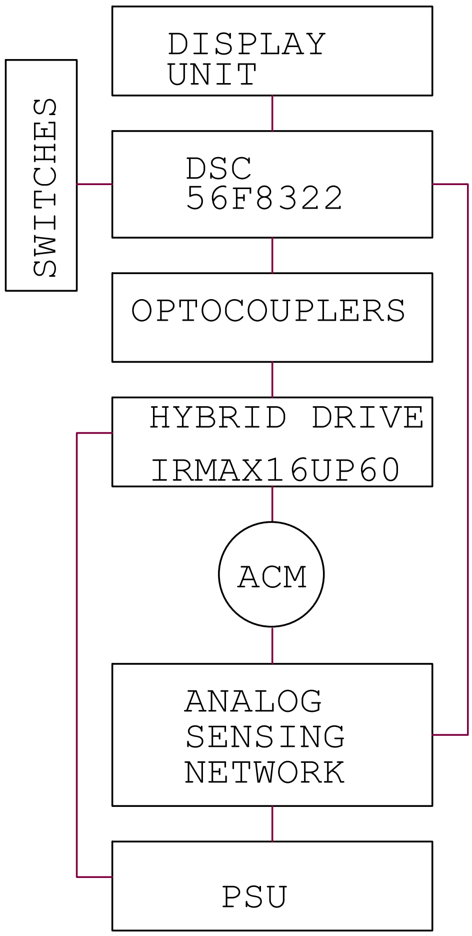

Fig.1 *Concept of the system*

After this verification a model that incorporates some imperfections of the environment was set. With this model, the steering pulses were time shifted and the calculations showed that the power dissipation is rising to a much higher level.

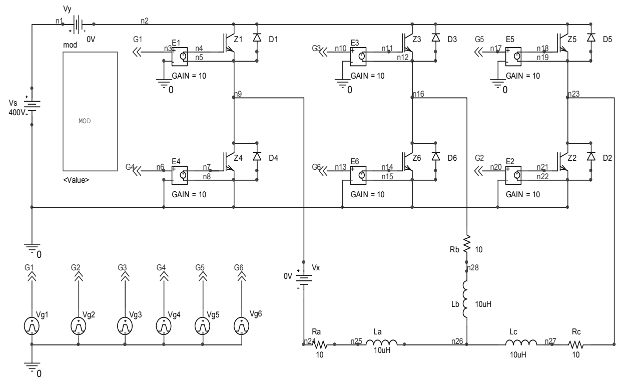

Fig.2 *Simulation model of the output stage*

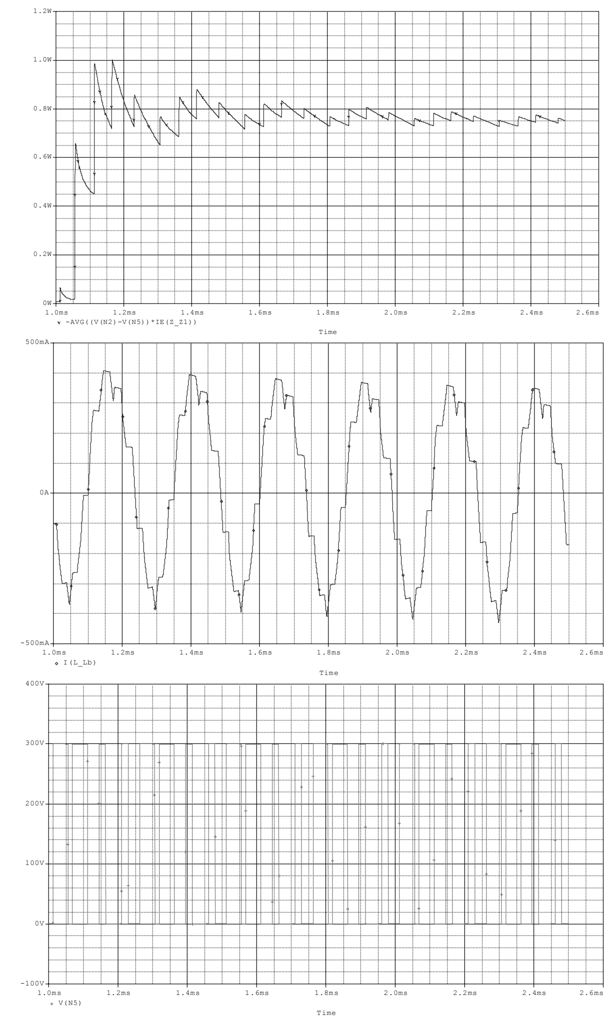

Fig.3 *Typical waveforms of the output stage, average power dissipation, single phase current and drive voltage waveforms*

At the beginning this was not considered as a real problem because the DSC was programmed to insert a certain dead time. Practically in the peripheral unites of the DSC a special PWM module is present. There are a lot of configurational registers and it is possible to define the delays associated with each generated pulse. In order to check the situation in the actual design some measurements were performed. The first set of measurements were performed by using logic analyzer and the relative pulse positions were observed. When output of the DSC controller was observed, everything looked fine. It must be pointed out that these signals are present at the digital side of the designed unit. Due to galvanic isolation it is not possible direct measurement of signal present on both sides, so separate verification of isolated signals was performed. Signals inspected alone looked as it was expected, regarding the shape, but that came from the nature of the measurement that is assosiated with application of logic analyzer.

After this initial measurements, the analog oscilloscope was introduced, and the waveforms of the drive pulses were inspected. It turned out that some of the pulses have excessive jitter. From the observed waveshapes it was indicative that there was substantial increase in the rise time of the steering pulses after the optocoupler units. Also, this slower rise time was forcing the buffer circuit in metastable region for a very short time, but still long enough to produce output changes with uncertain transitions. This effect is illustrated on Fig.4, as a result of a simulation with variation of some parameters, but very similar waveforms were captured with an oscilloscope, set in accumulate mode. Further more, this weak drive signals were prone to external influence of the harsh environment, and this also affected the output pulse position.

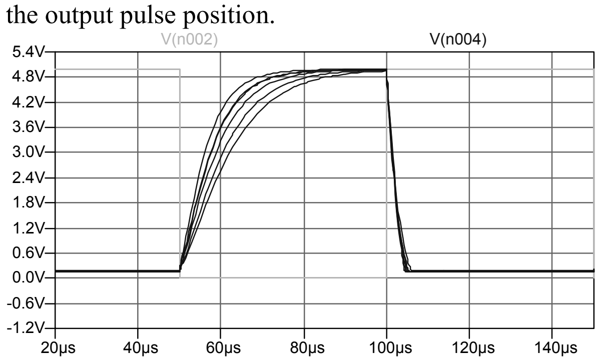

Fig.4 *Variation of the output pulses*

The detection of this phenomenon was not straightforward because the ground potential of the two blocks is not the same and some provisions have to be taken into account in order to avoid equalization current. Applying proper isolation with simultaneous measurement of the pulses infront and after the optocoupler both signals were inspected. The waveshapes indicated where the real location of the problem was. It was clear that the initial selection of the optocouplers was not the right one, because the guaranteed transition time via the optocoupler was not the only significant parameter. Actually, the selected optocouplers were of standard type, designed only with active pull down output configuration, open collector, while the high level was forced by the external pull up resistor. This type of optocouplers were also without Shottky diode inside, so they were entering region of deep saturation with non uniform recovery time.

3. SOLUTION OF THE PROBLEM

The first approach was to use higher values for the serial resistors in the diode drive section, in order to avoid extreme saturation of the output transistor, but this approach also affected the reliability of pulse transferring because of the limited value of CTR of the used optocouplers. Additionally the effect of variable duration of the drive pulses was observed. When the drive pulses with shorter duration are applied, then the output transistor within the optocoupler was entering the region of weak saturation. On the contrary, when this pulses were with longer duration, the transistor was entering region of deeper saturation, and the recovery time was different. This phenomenon was creating different rise time of the output pulses.

In the next step the initially selected optocouplers were replaced with new type devices that incorporate Shottky diode that prevents operation in the saturation region of the output transistor. This was proved as a successful solution to the detected problem of excessive power dissipation. Finally, optocouplers with different output stage were selected and they performed according to expectations. The finally selected model of the optocoupler has push pull drive stage and exhibits similar rise and fall times of the output drive pulses.

4.CONCLUSION

From this series of experiments we can conclude that no section of the designed circuit should be taken as granted, but rather each stage has to be verified, no matter how simple some stage might look like. Specially it is important to take care when digital signals are processed with non digital components, like optocouplers. Signals processed with such a components introduce distortion in the waveshape and in the timing characteristics of the signal, so it is important to inspect this signals with analog instruments rather then using logic analyzers only.

5. REFERENCES

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