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ASYMMETRIC SPACE VECTOR PWM FOR DUAL-INVERTER CONFIGURATION

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Abstract: *Dual two-level inverter topology is a simple structure capable to produce a multilevel voltage output equivalent to a 3-level inverter. Its modular structure consists of two standard two-level three-phase voltage source inverter (VSI) supplied by one or two dc sources. Known modulations cannot provide arbitrary power sharing between inverters in order to balance their dc voltages in case of two separate dc supplies. This paper proposes a space vector modulation (SVM) technique for a dual two-level inverter which can provide load control of the two dc sources as well as multilevel voltage output. An original modulation algorithm has been introduced to regulate the dc-link voltages of each VSI according with the requirement of a control system, by means of a specialized SVM. The proposed algorithm has been verified by experimental tests.*

Key Words: ***Multilevel systems/ Dual inverter/PWM***

1. INTRODUCTION

Multilevel inverters are increasingly used in high-power medium voltage applications due to their advantages compared to two-level inverters, such as lower common-mode voltage, lower dv/dt, lower harmonics in output voltage and current and reduced voltage on the power switches. Among numerous configurations a "dual" inverter consists of two inverters connected to open-winding load in order to obtain output voltage as a difference of corresponding leg potentials. Example in Fig. 1 shows two identical two-level three-phase inverters forming dual two-level inverter, however in general two inverters do not have to be equal with respect to type (VSI/CSI), number of levels, dc voltage value and voltage/current ratings [1]. The hardware simplification is significant compared with its neutral point clamped three-level inverter counterpart, due to use of readily available standard two-level inverters [2].

Dual-inverter topology was first reported twenty years ago [3] and remained interesting to the present day, due to its benefits such as:

1) Doubled output voltage – for given V_{dc} as supply output voltage amplitude reaches $4V_{dc}/3$ comparing to $2V_{dc}/3$ of standard single three-phase inverter with star-connected load.
2) Multilevel output voltage with up to nine-output voltage which is almost double compared to five-level output of standard single three-phase inverter with star-connected load. This feature provides lower ripple and dv/dt which can be important for high-power converters.
3) Doubled switching frequency compared to single inverter, since both inverters are modulated within switching period.

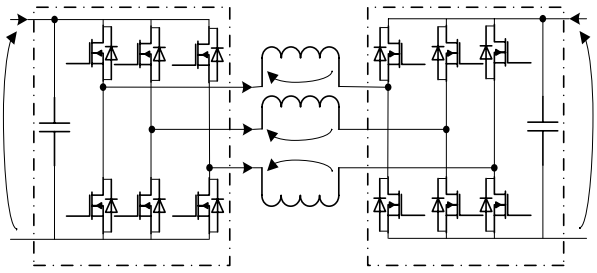


Fig. 1. *Dual inverter with two separate sources*

With reference to Fig. 1 it should be noted that is possible to work with single-supply with mandatory elimination of zero-sequence current component [3]. However, when the dc source can be easily split in two insulated parts, as for batteries and PV panels it is a simpler solution, as considered in the paper.

The quality of the output voltage is determined by the modulation algorithm and requires minimization of harmonic content, dv/dt and number of switching. Although converter can be modulated in closed loop mode such as in [3], here the focus will be on open-loop pulse-width modulation (PWM) control techniques impressing voltages to the ac side. The most commonly such methods are carrier based (CB) and space vector modulations (SVM). In [4] first CB modulation was proposed, providing the output waveform equivalent to 3-level inverter (e.g. neutral point clamped), with halved dc-voltage rating. Known modulations for dual inverter presume ideally symmetrical sources and consequently provide a symmetrical power sharing between them. In this paper a new modulation technique is presented, which provides maximum available output voltage and is able both to perform multilevel operation and to regulate the load power sharing between the two dc sources within each switching period.

2. DUAL INVERTER TOPOLOGY

Three-level inverters are a good tradeoff solution between performance and cost in multilevel converters for both medium and high-power applications. The main advantages of three-level inverters over the standard two-level ones are: reduced voltage ratings for the switches, good harmonic spectrum (making possible the use of smaller and less expensive filters), and good dynamic response. In particular, the waveform of the converter output phase voltage has up to nine levels. However, the control complexity increases compared to conventional voltage-source inverters (VSI). The presence of two insulated dc sources inherently prevents the circulation of common-mode currents, avoiding the use of an additional three-phase common mode reactor.

With reference to the scheme of Fig.1, using space vector representation, the output voltage vector $\bar{v}$ of the multilevel converter is given by the contribution of the voltage vectors $\bar{v}_H$ and $\bar{v}_L$, generated by inverter H and L respectively,

$$\bar{v} = \bar{v}_H + \bar{v}_L \tag{1}$$

$$\bar{v}_H = (2/3)V_H(S_{1H} + S_{2H}e^{j2\pi/3} + S_{3H}e^{j\pi 4/3}) \tag{2}$$

$$\bar{v}_L = -(2/3)V_L(S_{1L} + S_{2L}e^{j2\pi/3} + S_{3L}e^{j4\pi/3}) \tag{3}$$

where $\{S_{1H}, S_{2H}, S_{3H}, S_{1L}, S_{2L}, S_{3L}\} = \{0, 1\}$ are the switch states of the inverter legs. The combination of the eight switching configurations for each three-phase inverter (Fig. 2) yields to 64 possible switching states. If the two dc voltages are the same, i.e. $V_H = V_L = V_{dc}$, these switching states correspond to only 19 different output voltage vectors, including zero vector, as represented in Fig. 3. The redundancy of switching states represents a degree of freedom which is useful to develop a modulation strategy able to regulate the power sharing between the two dc sources within each switching period, as it will be shown later.

The reference output voltage $\bar{v}^*$ can be synthesized as the sum of the voltages $\bar{v}_H^*$ and $\bar{v}_L^*$ generated by the two inverters, as expressed by (1). Being the converter supplied by two separated sources, in several applications it is necessary to regulate the power flow from the sources. This requirement can be demanded in order to equalize the state of charge of two banks of batteries, or to exploit the different characteristic of two sources, e.g., generators and batteries. A possible approach to achieve the power sharing control is to define the decomposition of the total reference into two collinear vectors (Fig. 4):

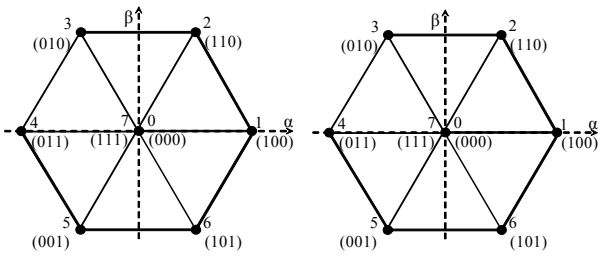


Fig. 2. *Eight switching states available from inverters H (left) and L (right)*

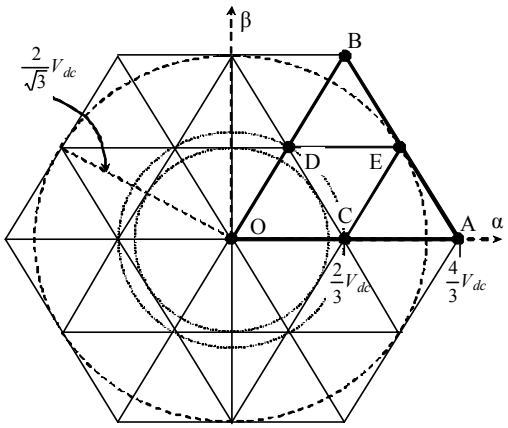


Fig. 3. *Dual inverter voltage vector plot in the case $V_H = V_L = V_{dc}$.*

$$\begin{cases} \bar{v}_H^* = k\,\bar{v}^* \\ \bar{v}_L^* = (1-k)\,\bar{v}^* \end{cases} \tag{4}$$

The condition expressed by (4) allows maximum dc voltage utilization. Being the output ac current of the two inverters the same, the coefficient k also defines the power sharing between the two inverters. In terms of averaged values within the switching period, the output power can be expressed as

$$p = \frac{3}{2}\bar{v}^*\bar{i} = p_H + p_L \tag{5}$$

where p_H and p_L are the individual powers from the two inverters. Combining (4) with (5) leads to

$$\begin{cases} p_H = \dfrac{3}{2}\bar{v}_H^* \cdot \bar{i} = k\,p \\ p_L = \dfrac{3}{2}\bar{v}_L^* \cdot \bar{i} = (1-k)\,p \end{cases}, \tag{6}$$

showing that p_H and p_L can be controlled by the control system. It should be noted that the coefficient k has a limited variation range depending on the value of the reference output voltage $\bar{v}^*$. For k = 0.5 two voltages and consequently powers are equal, and it represents a limit when voltage reference is equal to maximum available voltage. Furthermore, it has to be verified that both references are within the range of achievable output voltages of each inverter, depending on their dc voltages. In the case of a single inverter topology, if the voltage demand exceeds available dc voltage, the output voltage is simply saturated. With the dual inverter configuration, total voltage reference needs to be satisfied, so in case of voltage saturation of one inverter, the second has to provide for the missing part.

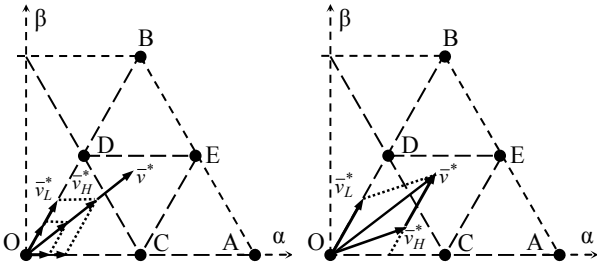


Fig. 4. *Power sharing capability collinear reference vectors (left) in contrast to general case (right)*

3. PROPOSED MODULATION

Once the inverter reference voltages $\bar{v}_H^*$ and $\bar{v}_L^*$ are determined by control system, they must be synthesized by the dual inverter and applied to the open-end windings of the transformer. Despite existence of CB algorithms e.g. "phase opposition disposition" approach for traditional three-level inverters [5], they are based on symmetry and hardly extendable to provide asymmetrical load of the sources. Therefore only SVM will be considered as a possible solution.

A simple SVM solution is to fix switching configuration of the one inverter and to modulate only other, as was proposed in [6], (fixing one inverter output is called "clamping"). The main advantage of the method is simplicity, e.g. it can be easily extended to more complex asymmetrical configurations (two inverters with different configurations/ratings) [7]. However it is easy to conclude that switching frequency of the output voltage is not doubled, still single inverters work with only half of the frequency having lower losses. Another significant drawback of the proposed solution is double instantaneous commutation that occurs when single inverters swap their roles for voltage reference in outside inner hexagon (Fig. 3). Furthermore this method cannot provide voltage output as demanded by (4) since output of the one inverter is not collinear to the other. The first solution, based on space vector approach, providing asymmetrical load has been proposed in [8]. However, it leads to switching sequences difficult to implement on the PWM generation unit of a standard (digital signal processor) DSP. Namely PWM unit can provided maximum one commutation in each switching half-period, which is not the case for voltage vector reference in intermediate triangle CDE (Fig. 2).

The principle of the proposed method is similar to SVM for a standard three-phase inverter. The voltage "hexagon" (Fig. 2) is divided in 6 equal sectors (triangles, like OAB), and further each sector is subdivided in four isosceles triangles (OCD, AEC, BDE and CED). The principle is explained for the first sector OAB and then analogously applied to other five cases. The switching sequences for the subsectors OCD, AEC and BDE are relatively easy to find and they provide symmetrical and discontinuous pattern (as shown in Fig. 5 for triangle AEC) [2]. The remaining subsector CED requires more complex solution with application of additional vectors in the switching sequence (Fig. 6). Obtained switching pattern will not be symmetrical anymore, except for some cases, in particular $k = 0.5$.

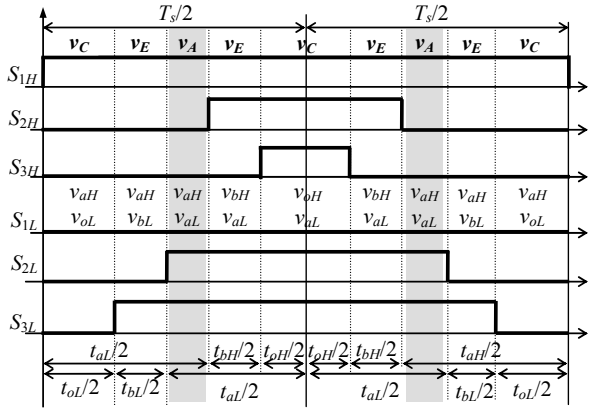


Fig. 5. *Switching sequence for the outer triangle AEC*

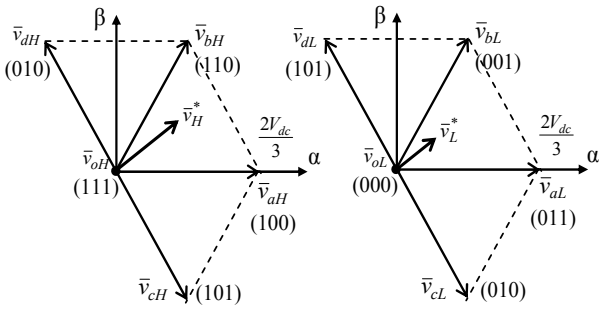


Fig. 6. *Introduced vectors $\bar{v}_{cH}$ and $\bar{v}_{cL}$ applied in the case of the intermediate triangle*

The proposed switching sequence, suitable for the implementation on a standard DSP is shown in Fig. 7. It adds two new vector combinations $(\bar{v}_{cH}, \bar{v}_{bL})$ and $(\bar{v}_{bH}, \bar{v}_{cL})$ equivalent to already present $(\bar{v}_{aH}, \bar{v}_{oL})$ and $(\bar{v}_{oH}, \bar{v}_{aL})$, as can be seen in Fig. 6. The application time t_c (denoted with grey) of the new vectors (Fig. 6) is introduced at the expense of zero vectors, and it present a degree of freedom. Another parameter is t_x (denoted with grey in Fig. 5) standing for a degree of freedom which determines the relative position of the switching sequence of the one inverter with respect to the other. When new vectors are expressed using the existing one can obtain:

$$\bar{v}_{cH} = \bar{v}_{aH} - \bar{v}_{bH}, \tag{7}$$

$$\bar{v}_{cL} = \bar{v}_{aL} - \bar{v}_{bL}. \tag{8}$$

giving

$$t_c \le \min\{t_{aH}, t_{aL}, t_{oH}, t_{oL}\} \tag{9}$$

From the figure the interval t_c need to satisfy the conditions:

$$t_c \le T_s/2 - (t_x - t_y) - t_{bH} \tag{10}$$

$$t_c \le T_s/2 - (t_{oL} - t_y) \tag{11}$$

It can be shown that:

$$0 \le T_s/2 - t_{bH} - t_x + t_y \tag{12}$$

$$0 \le T_s/2 - t_{oL} + t_y \tag{13}$$

therefore proving existence of non-negative t_c. The proposed switching sequence is discontinuous, and does not contain a simultaneous commutation of two legs.

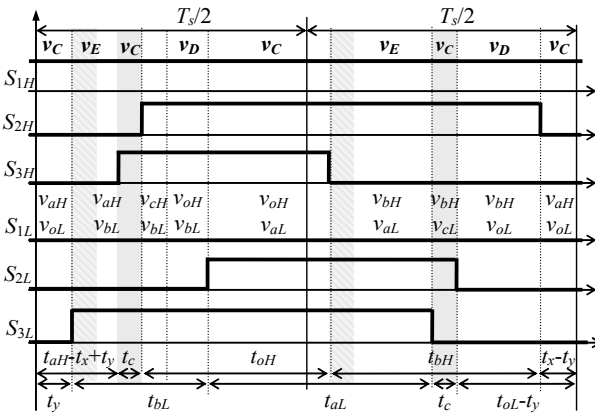


Fig. 7. *Sequence for the intermediate triangle CED*

4. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed modulation is implemented in TMS320F2812 DSP, equipped with two separate three-phase PWM units able to modulate two inverters and a 150 MHz timer. The experimental setup is shown in Fig. 8 with parameters in Tab. I. The experiment has been done for modulation index m = 0.75 and for both symmetrical (k = 0.5) and asymmetrical (k = 0.65) inverter's power sharing, with results presented in Fig. 9. Each PWM waveform is shown together with its fundamental component obtained by the low-pass filter. Figures 9(a) and 9(c) show individual phase voltages for each inverter. It can be noticed that voltages are in phase opposition in order to achieve maximum voltage utilization, as specified by (1) and (4). Figures 9(b) and 9(d) show corresponding total output voltages containing maximum nine output voltage levels, followed by its fundamental component. Note that in two cases both output voltages have equal fundamental component, only individual inverters provide different share, as stipulated by (4).

Table 1. *Main parameters of the converter*

INVERTERS	
configuration (H and L)	two-level VSI
MOSFETs (6 in parallel per switch)	IRF2807
MOSFETs ratings	V_{DSS}=75[V]; R_{DS}=13[mΩ]
dc-bus capacitance	23 [mF]
switching frequency	20 [kHz]
TRANSFORMER and GRID	
turn ratio	230/24 [V/V]
converter/grid-side winding connection	open ends/star
rated power	1500 [VA]
short circuit voltage	6.9 [%]
ac link inductance (converter side)	0.4 [mH]
grid voltage (line-to-line), frequency	250 [V], 50 [Hz]

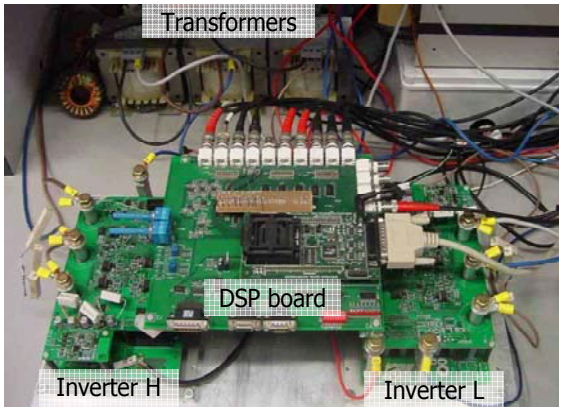
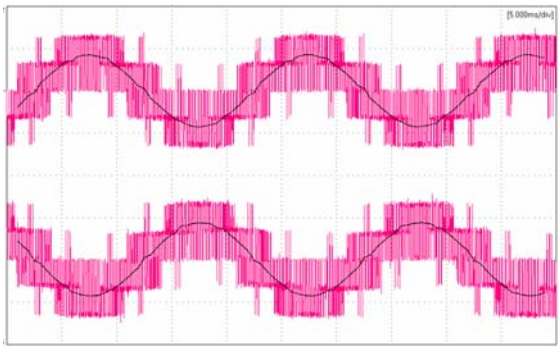


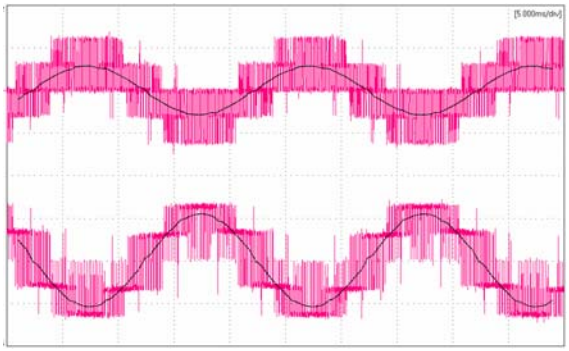
Fig. 8. *Dual inverter with two separate sources*

Another experiment proves the power ratio of the single inverters. The dual inverter works in a closed loop controlling dc voltage (as in active power filter application). In the first case, Fig. 10(a), the voltage reference decreases from 38 V to 30 V, approximately. This step leads to a sudden increment of the dc current from the dc source. In particular, the figure shows the time response of dc voltage and dc current for both the inverters. The second case, Fig. 10(b), is related to the opposite step of the voltage reference V_{dc}^{*}, from 30 V to 38 V, yielding to a sudden decrement of dc side power. Fig. 10 (b) shows the time response of dc voltage and dc current for both the inverters.

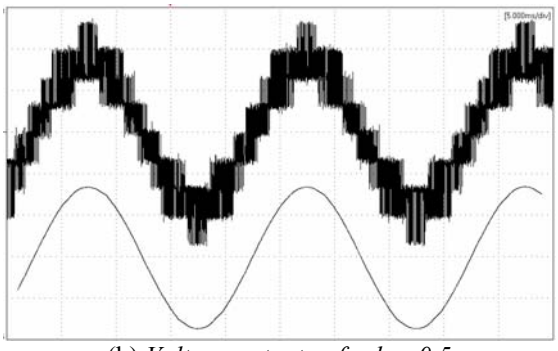
The provided experimental tests prove both proper multilevel waveform output and mutual ratio of the single inverter powers (4). A modified SVM algorithm has been adopted, having the merit to be easily implemented in industrial DSP controllers without the need of additional hardware (e.g. Field Programmable Gate Array).



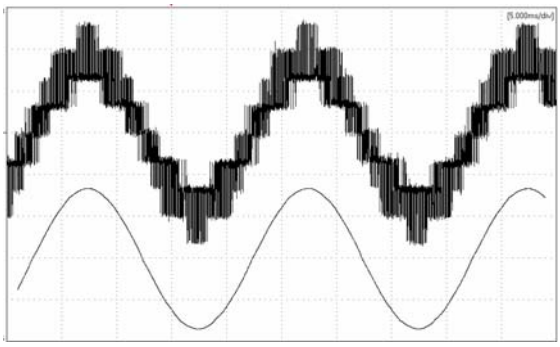
(a) *Single inverter voltages with fundamental for k = 0.5*



(c) *Single inverter voltages with fundamental for k = 0.65*

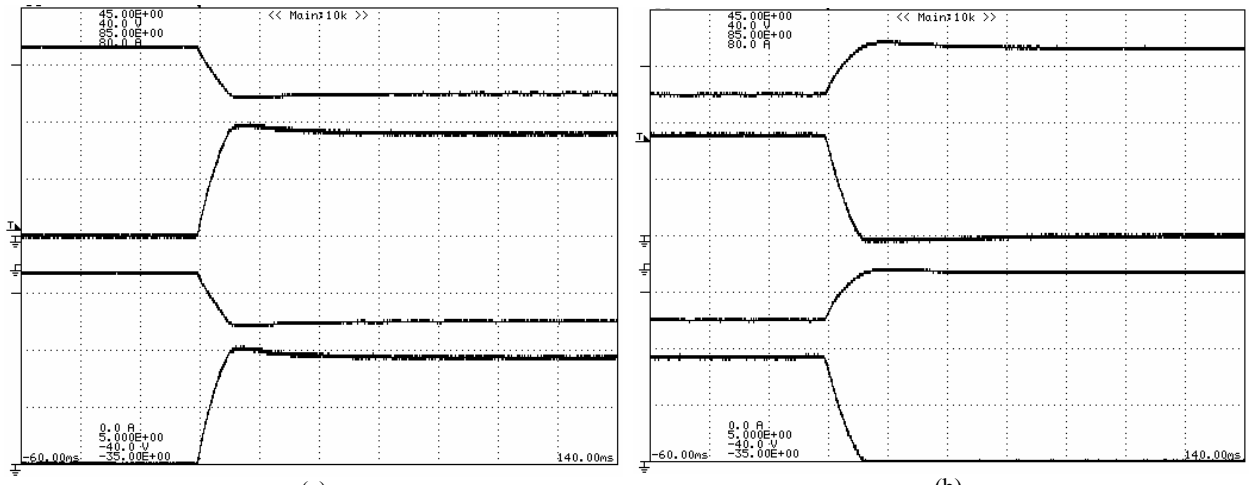


(b) *Voltage output v_l for k = 0.5*



(d) *Voltage output v_l for k = 0.65*

Fig. 9. *Voltage output v_l for m = 0.75 (5 ms/div, 20 V/div)*



(a) (b)

Fig. 10. C*hange of the reference dc voltage, V_{dc}^{*},(10 V/div, 35 V offset, 20 ms/div) and dc current (10 A/div) for both inverters, V_H, I_H, V_L, I_L (from top to bottom), voltage decrease (a) and increase (b).*

A. APPENDIX

The following inequalities need to be satisfied in order to prove the existence of time intervals for all vector combinations shown in Fig. 7. Starting from left-side of switching period inequalities are:

- $(\bar{v}_{aH}, \bar{v}_{oL}) \leftrightarrow \bar{v}_C$:

$$t_x / 2 \geq 0, \tag{A1}$$

- $(\bar{v}_{aH}, \bar{v}_{bL}) \leftrightarrow \bar{v}_E$:

$$(t_{aH} - t_x / 2) - t_x / 2 \geq 0 \tag{A2}$$

- $(\bar{v}_{oH}, \bar{v}_{bL}) \leftrightarrow \bar{v}_D$:

$$(t_x / 2 + t_{bL}) - (t_{aH} - t_x / 2) \geq 0 \tag{A3}$$

- $(\bar{v}_{oH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_C$:

$$(t_{aH} - t_x / 2 + t_{oH}) - (t_{bL} + t_x / 2) \geq 0 \tag{A4}$$

- $(\bar{v}_{bH}, \bar{v}_{aL}) \leftrightarrow \bar{v}_E$:

$$(t_{bH} + t_x / 2) - (t_{oL} - t_x / 2) \geq 0 \tag{A5}$$

- $(\bar{v}_{bH}, \bar{v}_{oL}) \leftrightarrow \bar{v}_E$:

$$(t_{oL} - t_x / 2) - t_x / 2 \geq 0 \tag{A6}$$

Conditions (A1)-(A6) lead to inequalities determining t_x.

$$\begin{cases} t_x \geq 0 & \text{(A7)} \\ t_x \geq t_{aH} - t_{bL} & \text{(A8)} \\ t_x \geq t_{oL} - t_{bH} & \text{(A9)} \end{cases}$$

$$\begin{cases} t_x \leq t_{aH} & \text{(A10)} \\ t_x \leq T_s - t_{bH} - t_{bL} & \text{(A11)} \\ t_x \leq t_{oL} & \text{(A12)} \end{cases}$$

On the basis of (A7)-(A12), the solution for t_x exists if the following condition is satisfied

$$\max\{0, t_{aH} - t_{bL}, t_{oL} - t_{bH}\} \leq \min\{t_{aH}, T_s - t_{bH} - t_{bL}, t_{oL}\} \tag{A13}$$

Inequality (A13) can be proved by verifying, one by one, the nine possible combinations of (A7)-(A9) and (A10)-(A12). As an example, for pair (A9) and (A10) the necessary condition is

$$t_{oL} - t_{bH} \leq t_{aH} . \tag{A14}$$

By introducing

$$t_{aH} + t_{bH} + t_{aL} + t_{bL} \leq T_s \quad . \tag{A15}$$

in (A14) yields

$$t_{oL} \leq T_s - t_{oH} \tag{A16}$$

which is true outside triangle OCD. A similar procedure can be used for the remaining combinations.

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