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A METHOD FOR COMMON MODE FILTER (CMMF) OPTIMISATION IN THE PWM INVERTER SUPPLIED MOTOR DRIVES

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Abstract: *The negative effects of PWM switch-mode inverters on the electrical motors, such as failures in the motor windings isolation and Electrical Discharge Machinery (EDM) leading to motor bearing failures are well known. Long cables between inverter and motor, very often found in, for example, railway applications, further increase these effects due to the cable reflections. The aim of this paper is to present an easy to use tool for practicing engineers providing mathematical analysis, design and optimisation of the LRC common-mode filtering network at the inverter output. This topology has been chosen after a literature research and considering the practical experiences with different CMMF topologies Firstly, a CMMF operation is explained, after that the filter is mathematically analysed using Laplace domain, leading to the definition of the filter optimisation criteria and in the end the simulation and experimental results are presented. This procedure was used on converters on different trains and has confirmed its value in operation.*

Key Words: ***Power Electronics / Drives / Common Mode Filtering***

1. THE NEED FOR THE COMMON MODE FILTER

The negative influences of PWM switch-mode inverters on the electrical motors are well known and well studied in the literature [8], [9], [13], [16], [17], [20], [23]:

- High values of phase/line voltage rise times (with IGBT inverter up to 6kV/µs) at the motor terminals cause the motor windings isolation to fail.
- High values of common-mode voltage rise times cause capacitive coupling effects in the motor to be pronounced, leading to electrical Discharge Machinery (EDM) and thus to motor bearing failures.
- Long cables between inverter and motor, often found in railway applications, further increase these effects due to the cable reflections.

Typical example of these effects can be found in the railway auxiliary loads, especially HVAC (Heating, Ventilation and Air-Conditioning) components are very sensitive. In order to eliminate them, a properly designed CMMF is necessary. Different common-mode filter topologies and the design methods have been presented in the literature [2], [3], [4], [5], [6], [10], [21].

Block diagram of a drive with a Common mode filter is presented in fig. 1. This filter topology was chosen according to literature recommendations [3], [6], [10], [16] and the practical experience the authors have gained during filter designs for the industry. CMMF consists of double LRC-network per inverter phase, clamping the inverter output to the DC-bus. In the case of decoupled inductors CMMF can be analysed in per-phase form.

Alternative topology is the one where the filter star-connection is clamped to the DC-bus middle. This topology, although having fewer components, is hardly to be recommended, because of the fact that DC-Bus middle point is seldom available and because of the voltage variations at the capacitive voltage divider. However, all the mathematical tools presented in the report are valid also for this topology, provided 50% of the DC bus voltage value has been taken into calculations.

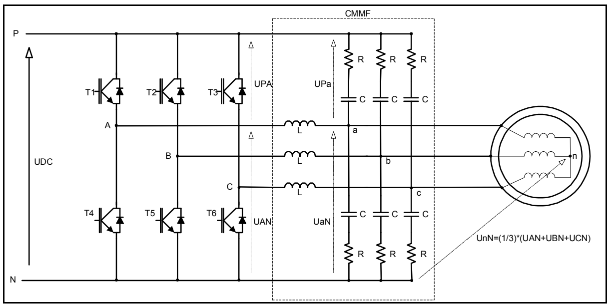

Fig. 1. *Common Mode Filter*

The aim of the CMMF is to limit both the voltage du/dt values on the motor phase/line terminals as well as in the Common Mode Voltage (CMV, U_{nN}).

In general case, the common mode voltage is defined as the voltage between the minus of inverter DC-bus and the, existing or virtual, star point of motor stator windings:

$$U_{nN} = \frac{1}{3}\left(U_{AN} + U_{CN} + U_{BN}\right) \tag{1}$$

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Motor phase voltages and motor line voltages can be defined as (without CMMF):

$$\begin{aligned} U_{An} &= U_{AN} - U_{nN} = U_{AN} - \frac{1}{3}\left(U_{AN} + U_{CN} + U_{BN}\right) \\ U_{Bn} &= U_{BN} - U_{nN} = U_{BN} - \frac{1}{3}\left(U_{AN} + U_{CN} + U_{BN}\right) \\ U_{Cn} &= U_{CN} - U_{nN} = U_{CN} - \frac{1}{3}\left(U_{AN} + U_{CN} + U_{BN}\right) \end{aligned} \quad (2)$$

$$\begin{aligned} U_{AB} &= U_{AN} - U_{BN} \\ U_{BC} &= U_{BN} - U_{CN} \\ U_{CA} &= U_{CN} - U_{AN} \end{aligned} \quad (3)$$

All the voltages of interest are thus influenced by inverter phase-to-minus voltages (U_{AN}, U_{BN}, U_{CN}) and from the Equations (1), (2) and (3) it becomes clear that in order to keep the motor voltage rise times under specified limits, it is necessary to limit the rise times between the filter outputs and the DC-bus minus (U_{aN}, U_{bN}, U_{cN}). Passive LRC network filters the inverter square-wave voltages as shown in fig 2, where Ts is the inverter switching period and D – duty cycle.

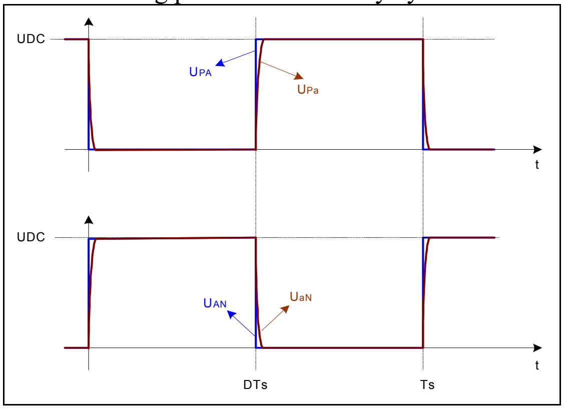

Fig. 2. *Voltages before and after the common mode filter*

The aim of this paper is to present an easy to use tool for practicing engineers providing mathematical analysis, design and optimisation of the common-mode filtering network at the inverter output. First, a CMMF operation is explained, after that the filter is mathematically analysed using Laplace domain, leading to the definition of the filter optimisation criteria and in the end the simulation and experimental results are presented. The presented optimisation method leads to the straightforward filter design procedure, enabling the du/dt values to stay below specified limits. In addition to that, the inclusion of the efficiency criterion minimises the CMMF power losses. This procedure was used on different converters on different trains and has confirmed its value in operation.

2. MATHEMATICAL ANALYSIS AND OPTIMISATION CRITERIA

The Common Mode Filter Transfer Function between inverter output and CMMF output can be written in Laplace domain as:

$$\frac{U_{aN}(s)}{U_{AN}(s)} = \frac{1 + sRC}{s^2 LC + sRC + 1} \quad (4)$$

Such a transfer function represents a typical form of the damped second order system, having additional positive zero:

$$W_s(s) = \frac{\omega_n^2}{z_1} \cdot \frac{s + z_1}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (5)$$

Where: ωn is the filter eigenfrequency, ζ – damping factor and z1 – system zero. Connection between equations (4) and (5) is:

$$\begin{aligned} \omega_n &= \frac{1}{\sqrt{LC}} \\ \zeta &= \frac{R}{2}\sqrt{\frac{C}{L}} \\ z_1 &= \frac{1}{RC} \end{aligned} \quad (6)$$

Frequency model of the system can be derived from (4), (5) as:

$$W_s(s) = \frac{\omega_n^2}{z_1} \cdot \frac{j\omega + z_1}{-\omega^2 + j\omega 2\zeta\omega_n + \omega_n^2} = \frac{1 + j\omega RC}{-\omega^2 LC + j\omega RC + 1} \quad (7)$$

2.1. Resonance and Reflection Criterion

Typical step response for the Ws(s) having different damping factor values is shown in fig. 3.

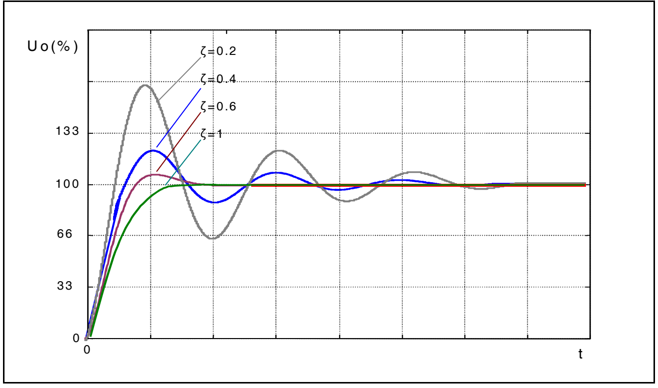

Fig. 3. *CMMF Step-Response for different ζ*

From (4)-(7) it is clear that in order to eliminate the overshoot and the possible system resonance, the damping coefficient ζ has to be greater or equal unity. It could be discussed that the condition ζ>0,707 also provides reasonable damping, however, the presence of the system zero (z1) causes additional overshoot (normally 5% minimmum) an therefore choosing ζ>1 is justified.

Thus the first optimisation criterion (Resonance Criterion):

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}} \geq 1 \Rightarrow R \geq 2\sqrt{\frac{L}{C}} \quad (8)$$

If the L/C ratio of the filter components is greater as L/C ratio of the cable, the cable reflections are also elliminated [6], [8], [13], [16]. It should be noted that all the filter components (R,L,C) are included in the resonace criterion.

2.2. du/dt Criterion

Since the role of the CMMf is to reduce voltage rise, it is necessary to provide a second criteria, taking into account optimal time-delay the filter can provide. Nominally, a dominant time-constant for a second order system as in (5) is defined as the time taking the system step-responce to achieve a 63% of the steady-state value, as shown in fig 4. From (5), (6) the system dominant time-constant can be expressed as:

$$T_d = \frac{1}{\zeta\omega_n} = 2\frac{L}{R} \quad (9)$$

Through this definition, it is possible to estimate the rise in the common-mode voltage in (V/µs) as:

$$\left(\frac{du}{dt}\right)_{CMM} = \frac{1}{3}U_{DC}\frac{0.63}{T_d}\frac{1}{10^6}\left(\frac{V}{\mu s}\right) \tag{10}$$

Factor (1/3) is due to the fact that the common-mode voltage steps are one-third of the DC-Bus voltage and the factor ($1/10^6$) is introduced because of typical (V/µs) definition of the acceptable du/dt values for the electrical motors.

In to keep order common-mode voltage rise-times under specified limits $(du/dt)_{CMMmax}$, the second optimisation criterion can be defined (du/dt Criterion):

$$\left(\frac{du}{dt}\right)_{CMM} \le \left(\frac{du}{dt}\right)_{CMM\max} \Rightarrow \frac{L}{R} \ge \frac{0.63\cdot U_{DC}}{3\cdot 2\cdot 10^6\cdot\left(\frac{du}{dt}\right)_{CMM\max}} \tag{11}$$

It is important to note that in this criterion, the capacitor value does not play any direct role, therefore, this criteria gives a relation between R and L.v

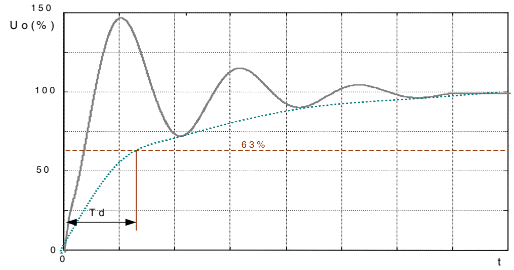

Fig. 4. *Dominant time-constant definition for the CMMF (or any second-order system)*

2.3. Efficiency Criterion

In order to optimise the CMMF efficiency, the power losses on the CMMF resistor have to be minimised. To obtain a plain mathematical model, the following simplification have been used (fig. 2.3.): It is supposed that the filter output voltages (U_{aN}, U_{bN}, U_{cN}) have a square-wave form. In reality they are less steep (fig. 3, (10), (11)), due to the CMMF action, but this simplification is nevertheless justified due to the fact that the square-wave voltages present the worst-case for the filter loss calculation.

Voltage on the capacitor and resistor can be calculated as:

$$u_C(t) = U_{DC}(1-e^{-t/RC}) \tag{12}$$

$$u_R(t) = U_{DC}\cdot e^{-t/RC} \tag{13}$$

where RC=τ is the voltage time-constant. From (13) and the fig. 5 it is clear that in order to minimize the resistor power loss, the voltage time-constant has to be made sufficiently small (for example: 3τ<< 0.5Ts). Power loss at resistor equals:

$$p_R(t) = \frac{u_R^2(t)}{R} = \frac{U_{DC}^2}{R}\cdot e^{-2t/RC} \tag{14}$$

In the case of small voltage time-constant (5τ≤ 0.5Ts), average power loss can be calculated as:

$$P_R = \frac{1}{T_s}\int_0^{Ts} p_R(t)dt = \frac{1}{T_s}\int_0^{3\tau}\frac{u_R^2(t)}{R}dt = \frac{1}{2}C\cdot U_{DC}^2\cdot f_s\cdot(1-e^{-6}) \tag{15}$$

where fs=1/Ts is the inverter switching frequency.

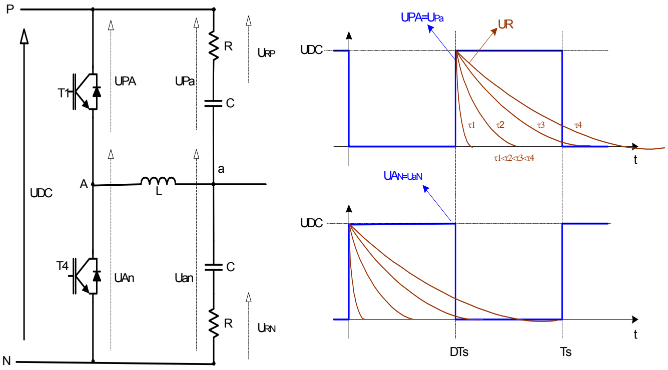

Fig. 5. *Voltages on the CMMF Resistors*

In the case of long time constants, the above integral goes up to 0.5Ts (however, this case is not of interest for filter design, since long voltage time constants lead to high resistor dissipation values and they are to be avoided since they minimise the filter efficiency):

$$P_R = \frac{1}{T_s}\int_0^{Ts} p_R(t)dt = \frac{1}{T_s}\int_0^{0.5Ts}\frac{u_R^2(t)}{R}dt \tag{16}$$

From the equation (15) can be concluded that the CMMF dissipation primarily depends on the capacitor value. Thus, the Efficiency Criterion:

$$C < C_{\max} = \frac{2\cdot P_{R\max}}{U_{DC}^2\cdot f_s\cdot(1-e^{-6})} \tag{17}$$

where the $P_{R\max}$ is the maximum tolerable dissipation on the CMMF.

3. FILTER DESIGN

In order to design a CMMF, all four criteria have to be taken into account and the appropriate design procedure would be:

1. Determine maximum power dissipation $P_{R\max}$
2. Determine maximum value for C according to the Efficiency Criterion (17)
3. Determine the voltage time-constant RC maximum value according to (3RC≤ 0.5Ts)
4. Determine minimum value for the L/R ratio according to the du/dt criterion (11)
5. Determine the damping value greater 1 according to resonance criterion (8)

It can be noted that this is an optimisation problem, where different sets of solutions can be obtained. The minimum price value has to be added when designing such a system.

From the designer point of view it is also important to note that:

1. CMMF inductor (L) has to be designed for the complete load current (complete load power rating plus ripple) and should be able to withstand at least the DC bus voltage
2. CMMF Capacitor (C) has to be of a “Snubber C” type, because of the high current/voltage stress and should be able to withstand at least the DC bus voltage with its tolerances

CMMF Resistor (R) has to be capable of managing the pulse-type loads as defined in (17) and should be able to withstand at least the DC bus voltage with its possible tolerances.

4. EXPERIMENTAL RESULTS

All Experiments were performed on a refurbishment project for New York Transit Authorities APS (UR NYCTA 13200) with 3.6kHz switching frequency and nominal power of 13.2kW. DC Bus voltage was set to be U_{DC}=665V...670V. For the motor-load experiments an 11kW induction motor with cosΦ=0.8 was used. Comparison between experimentally measured and analytically calculated common-mode voltage du/dt values and filter losses is given for each CMMF parameters (RLC) set.

Figures 6. and 7. show that the inverter output voltages without a common-mode filter have very high du/dt values, of approximately 6kV/μs and 5kV/μs respectively, which can lead to motor failure (isolation breakdown or EDM effects). Figures 8., 9. and 10 show results with the following filter parameters: L ≈450μH (500 μH), R=560Ω, C=0.47μF. A motor load was used, presenting a HVAC compressor in a train, since it is the most du/dt sensitive load.

These filter parameters, which were calculated useing usual CMMF design procedures, i.e. without the efficiency criteria, present one of the common mistakes in CMMF design. The passive components do tend to minimise the du/dt effects on the load, but they have high losses, leading to the increased system cost and volume, and also to a shorter CMMF life time, because of the increases losses and thus temperature.

As it can be seen from fig. 11 the power losses are unacceptably high. According to efficiency criteria, the use of smaller capacitor value is a must.

In order to minimise the CMMF losses and at the same time to keep voltage rise-times under limits, a smaller capacitor value was chosen according to efficiency criteria. Following experiments were made with: L ≈450μH (500 μH), R=560Ω, C=0.01μF, again with the compressor load. The following figures show that the losses were minimised 18 times, while the du/dt values remained the same. Again, the calculated and the experimental values are in accordance as it was the case with calculated and simulated values.

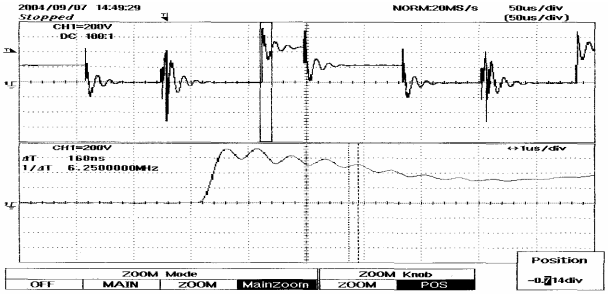

Fig. 6. *Motor Phase Voltage without CMMF, du/dt≈6000V/μs*

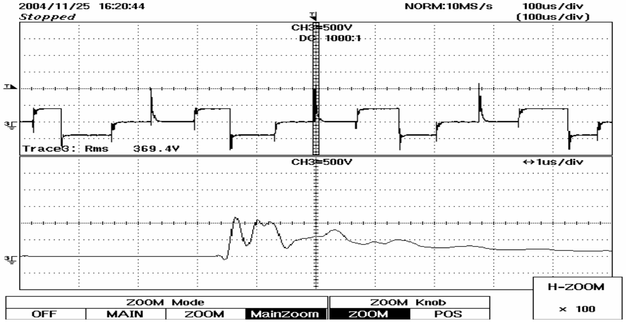

Fig. 7. *Motor Common-Mode Voltage without CMMF, du/dt≈5000V/μs*

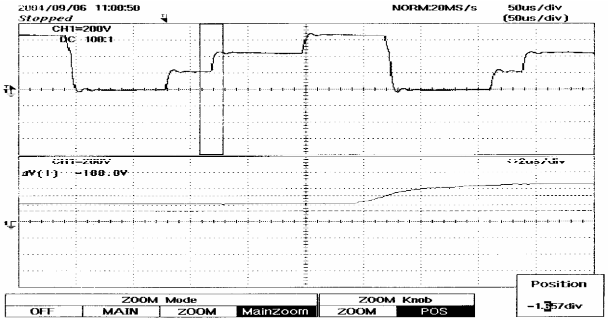

Fig. 8. *Common Mode Voltage du/dt≈100V/μs (Calculated du/dt≈80 V/μs)*

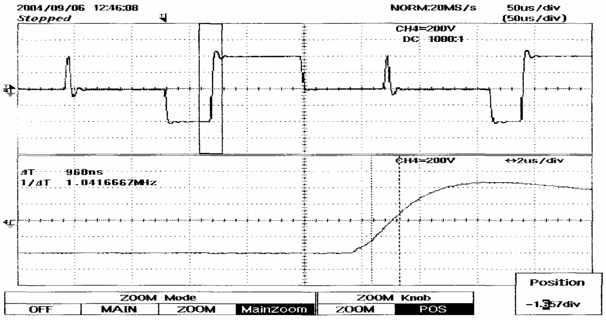

Fig. 9. *Phase-to-Phase Voltage du/dt≈155V/μs (Calculated du/dt≈160 V/μs)*

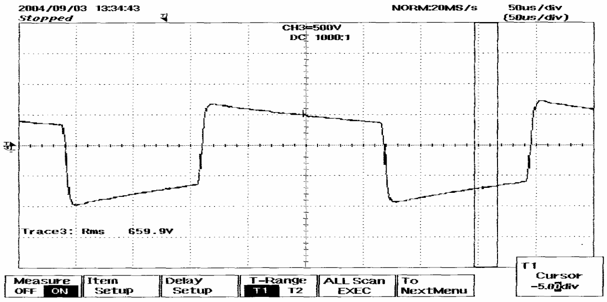

Fig. 10. *Voltage on CMMF Resistor, Losses P_R≈200W (Calculated P_R≈220W)*

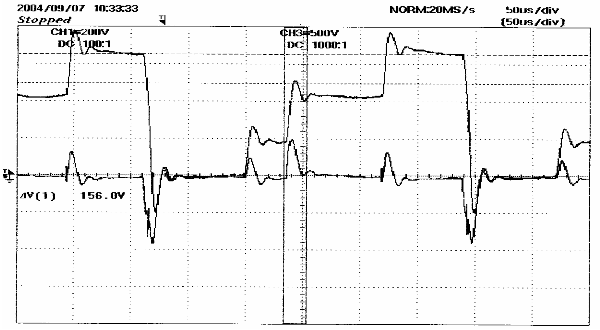

Fig. 11. *Common Mode Voltage (Upper Trace) and Voltage on CMMF Resistor (Lower Trace), du/dt≈78V/μs (Calculated du/dt≈80V/μs), Losses P_R≈11W (Calculated P_R≈10W)*

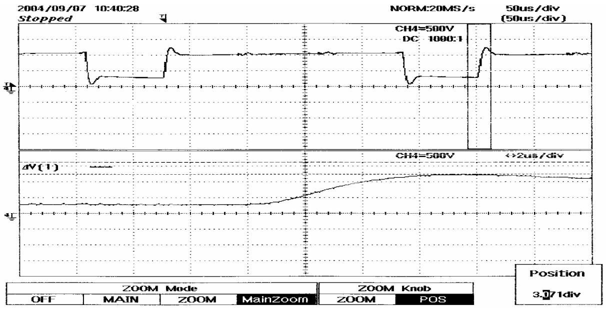

Fig. 12. *Phase-to-Phase Voltage du/dt≈130V/μs (Calculated du/dt≈140 V/μs)*

5. CONLUSION

This paper presented an easy to use tool for practicing engineers providing mathematical analysis, design and optimisation of the LRC common-mode filtering network at the inverter output. Such system minimises du/dt values both in the phase/line voltages and in the common mode voltage. It was shown that by using three criteria:

- Resonance/Reflexion criteria
- Rise-Time criteria
- Efficiency criteria

an optimised solution for CMMF design can be found. The presented optimisation method leads to the straightforward filter design procedure, enabling the du/dt values to stay below specified limits. In addition to that, the inclusion of the efficiency criterion minimises the CMMF power losses. In order to justify the design procedure, extensive simulations and experiments were performed and the results supported the theory. The same procedure was afterwards used on converters on different trains and has confirmed its value in daily operation.

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