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IMPROVED THREE-PHASE CURRENT RECONSTRUCTION USING SINGLE CURRENT SENSOR TECHNIQUE

Evgenije Adžić[1,2], Milan Adžić[3], Darko Marčetić[1], Zoran Ivanović[1,2], Nikola Čelanović[1,2]

[1]University of Novi Sad, Faculty of Technical Sciences, Novi Sad, Serbia
[2]Typhoon HIL, Inc. Cambridge, USA, Baden, Switzerland, Novi Sad, Serbia
[3]University of Novi Sad, College of Applied Sciences, Subotica, Serbia

Abstract: *This paper illustrates the method for three-phase current reconstruction in pulse-width modulated (PWM) voltage source converters using a single current sensor in DC link. Specially, certain conditions are indicated when current reconstruction is distorted due to the too narrow current pulse width and ripple in DC link sensor. To solve this problems, paper proposes modified PWM and improved DC link current sampling scheme. Proposed single current sensor technique is realized on control platform based on the TMS320F2812 DSP processor. Thanks to an Ultra-Low Latency (ULL) hardware-in-the loop (HIL) emulator, the proposed algorithm, its implementation on a DSP processor, code optimization and "laboratory" testing were all merged into one development step.*

Key Words: ***AC motor drives, PWM inverter, current measurement, single current sensor, hardware in the loop.***

1. INTRODUCTION

The persistant cost reduction and robustness increase demand of the general-purpose AC drives pushed into the background their high and optimal performances. From this point of view it is necessary to offer to the market, general-purpose drive that is produced in mass series, which has a very small production and the market price and that is highly reliable. A large number of sensors, harnessing cables and expensive signal-conditioning circuitry deteriorate its reliability and boost the system price, and therefore is highly unacceptable. In high-reliability and cost-critical drives applications the shaft sensor should be eliminated first, using one of the numerous shaft-sensorless methods [1], [2]. All of the proposed methods base the motor speed estimation on motor terminal voltage references and measured motor currents. An alternative reliable and low-cost solution for current measurement is to use a single current sensor that measures DC link current only, and to perform an on-line reconstruction of all three motor line currents [3].

Various approaches for current reconstruction have been proposed in relevant literature [4]-[7]. The method described in this paper can achieve an effective dc current measurement by altering the three-phase PWM voltage patterns sufficiently, if longer active vectors and DC link current width are needed. PWM signal shifting is done as needed maintaining reference average value and having the least possible impact on original PWM pattern. Another problem in the application of single current sensor scheme is a occurance of offset jitter like waveform error in the reconstructed line currents due to the inevitably non-synchronized DC link current sampling and the PWM current ripple. It directly reflects on current vector components in stationary (α-β) and synchronous (d-q) reference frame, which can deteriorate complete drive control. The paper proposes modified PWM pattern control and DC link current sampling scheme in order to elliminate and remove this kind of waveform error in current reconstruction process.

The inverter topology and the relationship between the DC link current, the output line currents, and the voltage vectors are defined first. Next, the problematic issues related to the DC link current sensor technique, including unobservable low modulation index operation, partially observable sector transition instances, and offset jitter like waveform error are discussed. An implementation of solution which overcomes these problems is presented and test results obtained using hardware in the loop emulated induction motor drive are given and analyzed.

2. THREE-PHASE CURRENT RECONSTRUCTION USING SINGLE CURRENT SENSOR IN DC-LINK

The most economic way for three-phase motor line currents measurement is to use only one shunt resistor (R_{shunt}) placed in the inverter dc circuit, as shown on Fig.1. In this section we make the results comparison.

The link between the measured dc-link current (i_{DC}) and the motor line currents (i_a, i_b, i_c) depends on the states of inverter switches (*T1-T6*). There are six switch state combinations that give active voltage vector (*V1* –

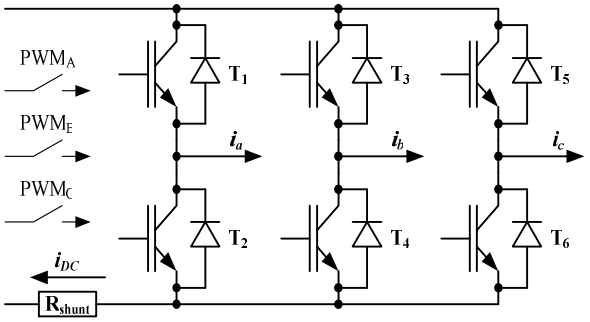

Fig. 1. *Three-phase voltage inverter with single dc-link shunt resistor.*

V6), and two resulting in non-active or zero vectors (*V0* and *V7*). During the application of non-active vectors dc-link current is always zero, while during the application of active vectors it is always related to one of the line current, as shown on Table 1. Due to the complementary switching mode, voltage vectors are defined using switching functions of upper switches only, for example *V1*=100 means *T1*= ON, *T3*= OFF, *T5*= OFF (i.e. *PWMA*=ON, *PWMB*=OFF, and *PWMC*=OFF, respectively).

Typical 3-phase PWM period contains two active voltage vectors that are used long enough for currents reconstruction, as shown in Fig 2. The figure shows three PWM signals for the voltage vector in the first sector (k=1), in which phase A has the highest, and phase C the lowest voltage command.

There are two active vectors, vector *V1* (V_k) with vector time *T1* (T_k), and vector *V2* (V_{k+1}) with vector time *T2* (T_{k+1}). During the remaining time in the PWM period zero vectors are applied ($T0 = T_{PWM} - T_k - T_{k+1}$) and there is no current flowing in the dc circuit, as shown in the Fig. 2. The PWM on-times for each phase are calculated based on the voltage vector times and number of the current sector. For example, in sector 1 is valid:

$$PWMA = T_{\mathrm{LONG}} = \frac{T_0}{2} + T_1 + T_2$$

$$PWMB = T_{\mathrm{MIDDLE}} = \frac{T_0}{2} + T_2$$

$$PWMC = T_{\mathrm{SHORT}} = \frac{T_0}{2}$$

During each of two active voltage vectors, one motor line current can be sampled (Table I). Since the sum of all three line currents flowing to the motor must be zero, measuring the two line currents allows a determination of the remaining third motor line current, which stays unobservable during the entire PWM period.

TABLE I
RELATIONSHIP BETWEEN DC AND MOTOR LINE CURRENTS

$V_0 = 000 \rightarrow i_{DC} = 0$	$V_4 = 011 \rightarrow i_{DC} = -i_a$
$V_1 = 100 \rightarrow i_{DC} = +i_a$	$V_5 = 001 \rightarrow i_{DC} = +i_c$
$V_2 = 110 \rightarrow i_{DC} = -i_c$	$V_6 = 101 \rightarrow i_{DC} = -i_b$
$V_3 = 010 \rightarrow i_{DC} = +i_b$	$V_7 = 111 \rightarrow i_{DC} = 0$

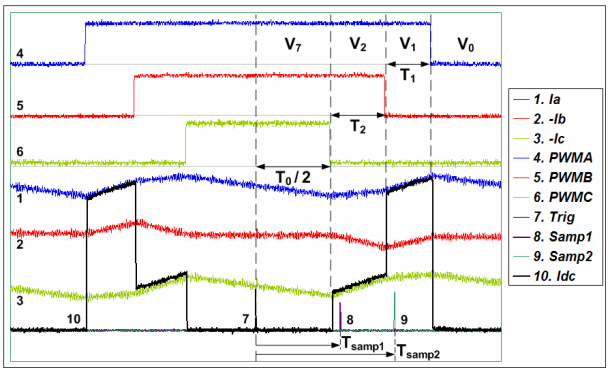

Fig. 2. *Three-phase PWM pattern with two active voltage vectors and corresponding dc-link current waveform. Sampling moments included.*

For three-phase current reconstruction idea to work, both dc-link current sampling instants must be precisely synchronized with PWM pulses, usually refer to begin or middle of PWM period (*Trig* signal in Fig. 2). Modern DSP already support this requirement, since they have synchronization lines between PWM and ADC peripherals and allow parallel triggered sampling at any instant within the PWM period. According to the Fig. 2, the optimal sampling instants should be calculated relatively to the active vector transition moments. However, for a reliable dc-link current reading, the signal sampling must take place after an additional, pre-calculated delay, T_{delay}:

$$\begin{aligned} T_{SAMP1} &= T_{\mathrm{SHORT}} + T_{delay} = T_{\mathrm{SHORT}} + T_{on} + T_r + T_s \\ T_{SAMP2} &= T_{\mathrm{MIDDLE}} + T_{delay} = T_{\mathrm{MIDDLE}} + T_{on} + T_r + T_s \end{aligned} \quad (2)$$

The sample delays include total switching device turn-on delay time (T_{on}), dc-link current measurement signal rise-time (T_r) and signal settling time (T_s). The T_{on} parameter includes dead-time that is automatically inserted by DSP, IGBT driver, PWM signal processing time and worst-case IGBT on-time delay.

Values of all delays involved in the dc-link current sampling process are of order of few μs, and indicates that only low-latency real-time emulator can provide adequate simulation accuracy.

3. PROBLEMS IN CURRENT RECONSTRUCTION STRATEGY

Practical difficulties with dc-link current measurement can occur when a PWM period holds active vectors that are present only for a short time, which happens in two common cases (Fig. 3). The first case is a low modulation index, when both active vectors are present for a short time. The second case occurs regardless of the modulation index, when the reference voltage vector passes near or falls on one of the six active vectors (i.e. transition between sectors), and produces at least one short active vector. During these situations, the method may be unable to reliably measure and calculate the motor line currents.

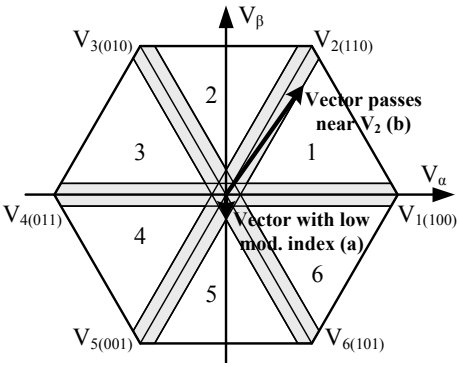

Fig. 3. *Areas in α-β frame in which current reconstruction is not possible.*

Therefore, it is desirable to use one of the suggested methods which achieve effective dc current measurement by modifying the three-phase PWM voltage patterns sufficiently, if longer active vectors are needed [4], [5]. Otherwise, one can estimate motor line currents during non-measurable periods without modifying the PWM pattern, using mathematical machine models and the reference voltage vector information [6]. The observer-based methods are more complex and computationally intensive, and therefore it is more preferable to use simple and robust modified PWM scheme.

In this paper such PWM scheme, which shifts PWM signals in order to account cases where reliability of the dc current measurement may be in question, is used. Fig. 4 shows applied solution with recorded example where first active voltage vector in lagging side of the PWM period is less then a predetermined shortest active vector time or minimum dc current sampling window:

$$T_{\min} = T_{on} + T_r + T_s + T_{S\&H} \qquad (3)$$

where $T_{S\&H}$ is the minimum time during which the dc-link current signal has to be still present at ADC inputs after the sampling has initiated. Generally, the PWM signal associated with the phase having the middle voltage command (*PWMB*) is shifted to the right in order to form a sufficiently long ($=T_{min}$) first sampling window in lagging side of the PWM period. Then, the duration of the succeeding voltage vector is calculated and if needed the PWM signal associated with the phase having the highest voltage command (*PWMA*) is also shifted to the right in order to form a second sampling window. After the PWM signals are shifted, a dc-link current measurement can be reliably taken at the first possible instant. The sampling close to the beginning of short active vector would result in its minimum possible extension, and would give less impact on the current ripple and result in less audible noise. This makes sampling at earliest possible moment more favorable than sampling at the middle or the end of current sampling window, especially if low modulation index is used.

Precise PWM signals shifting method and correct alignment of the sampling signals with begin (middle or end) of the active vectors can be agreeable simulated and rapidly validated and verified only using ULL HIL connected to the real controller platform.

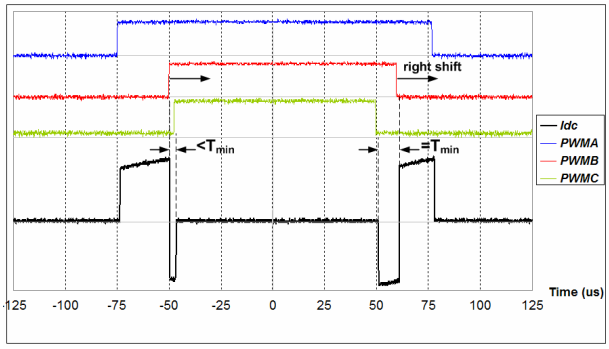

Fig. 4. *Modified PWM pattern: PWMB signal is shifted to right to form first sampling window wide enough ($=T_{min}$) for reliable current reading.*

Another problem reflects in the fact that regardless of the selected PWM shifting method for line currents reconstruction, the end results cannot be the line currents sampled in the middle of the PWM period. To make things even worse, two observable line currents cannot be sampled simultaneously, each is sampled when available and therefore with certain time-displacement between two samples. As a result, these two values are phase shifted differently from the middle point of PWM period, in which the average PWM value of the line current is located. A combination of time-displacement of the two line current samples and current PWM ripple produces a particularly shaped error of the reconstructed line current, as shown in Fig. 5.

From Fig. 5 it is clear that two abrupt excursions in the current signal can be expected during one period of fundamental output voltage. The ripple-induced error exhibits jumps of $3 \cdot \Delta$ amplitude twice per period (transitions between Sectors 1→2 and 5→6 for line current i_a), and it practically produces an offset section. For other two line currents, transition offsets would appear at different positions (1→2 and 3→4 for i_b and 3→4 and 5→6 for i_c current).

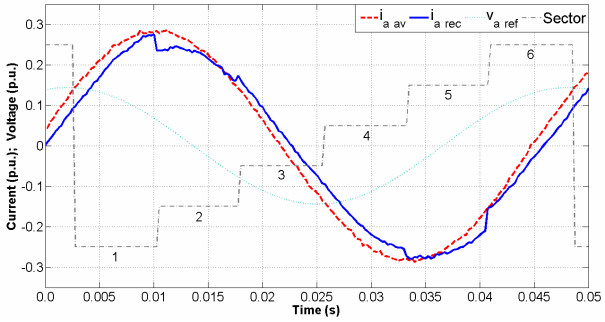

Fig. 5. *HIL and DSP experimental results – reconstructed line current samples (i_{a_rec}) in comparison to the line current average values during PWM periods (i_{a_av}). for light load operation and reduced motor flux (650rpm, 135Vrms, 5.7Arms).*

4. MODIFIED SCHEME FOR PWM AND DC LINK CURRENT SAMPLING

Fig. 6 shows dc-link current during two consecutive PWM periods and details related to proposed method for eliminating previously described error in the reconstructed currents waveforms. One can note that sampling signals (*Samp1* and *Samp2*) in a lagging half of the first PWM period are aligned to the end of the active

voltage vectors. *Samp1* and *Samp2* define sampling instants for recording line currents $-i_{1\_1}$ and i_{2_1}. Opposite, in a leading half of the next PWM period dc current is sampled at begin of the corresponding active vectors. There, sampling signals *Samp3* and *Samp4* define instants for recording line currents i_{2_2} and $-i_{1\_2}$, respectively. The line currents at the time instant t_c (0), representing average values in two consecutive PWM periods, can be obtained using simple calculation:

$$i_1(t_c) = -\frac{i_{DC}(T_{SAMP1}) + i_{DC}(T_{SAMP4})}{2} = -\frac{i_{1\_1} + i_{1\_2}}{2} \quad (7)$$

$$i_2(t_c) = \frac{i_{DC}(T_{SAMP2}) + i_{DC}(T_{SAMP3})}{2} = \frac{i_{2\_1} + i_{2\_2}}{2}$$

$$i_3(t_c) = -(i_1(t_c) + i_2(t_c))$$

One must note that three simultaneously measured line currents, $i_1(t_c)$, $i_2(t_c)$ and $i_3(t_c)$, are determined every two PWM periods based on four non-simultaneously sampled dc link currents. It remains to assign resultant currents i_1, i_2 and i_3 to motor line currents i_a, i_b and i_c depending on the actual sector number. Fig. 6 also includes situation that exist during sector transition, showing the details related to the PWM pattern used. *PWMA*, *PWMB*, and *PWMC* signals correspond to the originally symmetric PWM signals, when reference voltage vector passes from sector 6 to sector 1. In considered case, period of time that active voltage vector *V2* is applied needed for measuring $-i_{c\_1}$ and $-i_{c\_2}$ ($-i_{1\_1}$ and $-i_{1\_2}$) is not sufficiently long enough. Therefore, the PWM signals are modified which can be observed in *PWMAm*, *PWMBm* and *PWMCm* signals. In first PWM period (left in Fig. 6) and in its lagging side *PWMBm* is shifted right refer to *PWMB* signal. Similar, in the next PWM period (right in Fig. 6) and in its leading side *PWMBm* is shifted left refer to original *PWMB* signal in order to have reliable current reading.

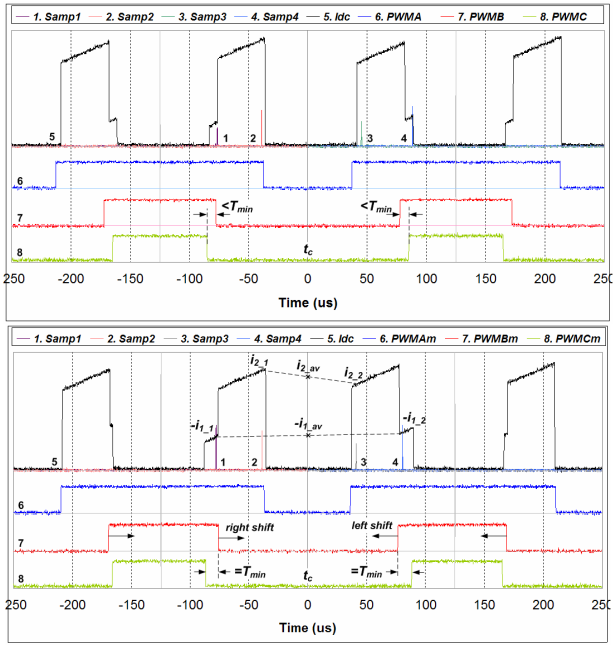

Fig. 6. *a) Proposed dc-link current sampling and original, naturally symmetrical PWM pattern. b) Proposed dc-link current sampling and modified PWM pattern for reliable and accurate line current reconstruction.*

5. TEST RESULTS

In the early stage of control algorithm development and further to confirm usefulness of proposed high-reliability current reconstruction method, new hardware-in-the-loop (HIL) platform was used.

In this paper, a high-fidelity ultra-low latency (ULL) HIL platform Typhoon HIL400 dedicated for testing and design of high-power electronics systems replaced real hardware setup. The used HIL platform comprises a programmable, application specific, processing architecture targeted to FPGA board with fast analog/digital input/output interfaces, and with accompanying software tool chain performing the function of power electronics circuit analyzer/compiler. Comprehensive details about the processor architecture and applied power electronics modeling/solver can be found in [8]. This approach provided real-time execution on the order of 1μs emulation time step including input/output interface latency. Therefore, from the controller point of view there is no distinction between the real-time control of the physical power electronics system and the HIL emulator.

ULL enabled setting up of high switching frequency as 4 kHz in the controller PWM unit, throughout all experiments in the paper. For this application HIL ULL property showed particularly helpful during control algorithm design, because its time-interrupt handling nature requires precise PWM signal shifting and fine alignment of sampling times inside the short PWM period of 250 μs. Standard off-line simulations are slow for simulating these issues and due to necessary simplifications could provide only a low level of functional faithfulness. Particularly, this application would show that ULL HIL Typhoon HIL400 represents irreplaceable tool for rapid and efficient modeling and testing power electronics embedded controllers and its interactions. Controller platform interfaced with the ULL HIL system, as shown in Fig. 7, is based on Texas Instruments DSP TMS320F2812.

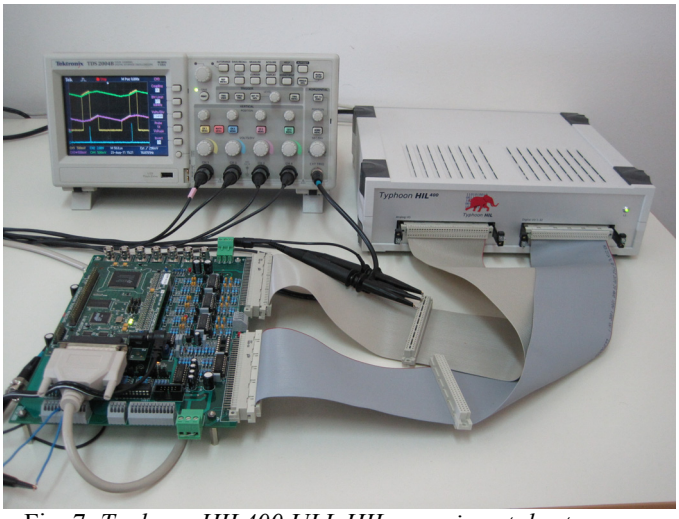

Fig. 7. *Typhoon HIL400 ULL HIL experimental setup with controller ezDSP TMS320F2812 and its interface board.*

For experiments an indirect vector control was implemented and used in speed control mode. The motor was lightly loaded (10% rated), which together with reduced rotor flux reference resulted in a low current r.m.s. value and in the significantly distorted reconstructed current waveforms.

The current waveforms results presented here were acquired for speed references of 650 rpm. Figs 8 and 9 illustrate reconstructed current waveform before and after proposed method modification, when measured line currents (i_{a_av}) are used as current feedback in control algorithm. Before modifications, the motor line current (i_{a_rec}) has extremely distorted waveform, with two jumps in opposite directions producing offset jitter like error lasting 1/3 of the fundamental period. The jumps occur at the 1→2 and 5→6 sector transitions, as predicted with explanation in chapter 3. The modified reconstructed line current ($i_{a\_rec\_corr}$) has a more sinusoidal waveform. The sudden offset in current waveform is hardly noticeable and the reconstructed currents are now closer to their mean PWM values (i_{a_av}). The resulting *d-q* currents are also improved (Fig. 9). Without the modification, the *d-q* currents (i_{d_rec} and i_{q_rec}) significantly oscillate around the average value (6th harmonic) and have wrong average values. An improvement reflecting the 6th harmonics reduce is particularly evident in *d*-current component.

The reason that measured currents are used as feedback signals is to indicate wrong average values of *d-q* currents obtained by current reconstruction method. However, better results are obtained with the proposed method, as especially recorded *q*-current components in Fig. 9 confirms.

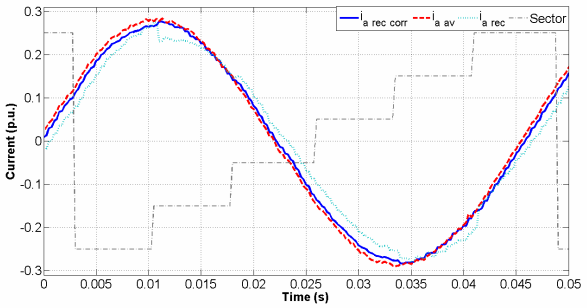

Fig. 8. *Reconstructed motor line current waveform without (i_{a_rec}) and with (i_{a_corr}) proposed modifications.*

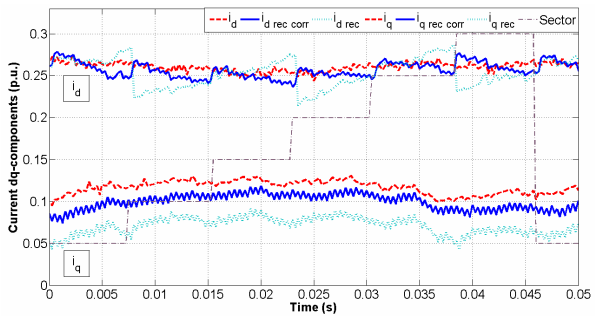

Fig. 9. *dq-current component waveforms without (i_{d_rec}, i_{q_rec}) and with ($i_{d\_rec\_corr}$, $i_{q\_rec\_corr}$) proposed modifications, compare to dq-current components of measured line currents (i_d, i_q) .*

6. CONCLUSION

Improved and reliable motor phase-current measurement using single dc-link current sensor have been proposed. The unusual waveform error present in reconstructed line current signals has been analyzed. The paper proposes a simple and robust scheme to cancel that error and boost the performance of AC motor drives. After the scheme was introduced, the additional offset and oscillations at sixth harmonic frequency in resulting d-q current components are reduced. As a result, the proposed scheme can be helpful in high-reliability and high-performance drives. This application specially confirmed that Ultra-Low Latency (ULL) Hardware-in-the-Loop (HIL) is particularly helpful and even necessary for efficient and rapid control algorithm development, because it enables design engineers to observe all the fine details: dc-link current, PWM signal shifting, change of sampling time moments inside the PWM period, relationship between line currents and dc-link current through the sectors, PWM current ripple influence, etc.

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