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TESTING OF PLL STRUCTURES ON REAL TIME SYSTEMS

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Abstract: *Recent market expansion of renewable energy sources gave a large number of different grid connected converters. Each of these converters needs a grid synchronization algorithm. This is by no means a new requirement, but for high-power, three-phase converters such algorithm is complex and requires a lot of time and resources to fully develop and test from ground up. This paper shows an alternative method for development, testing and selection of PLL structure which results with a ready-to-use code suitable for real-world grid-connected power converter.*

Key Words: ***Converters/PLL/Hardware in the loop***

1. INTRODUCTION

Although precise synchronization with grid voltage necessary for correct operation of grid-connected converters is a well known problem, this topic is still an active and prolific field of research. Modern synchronization algorithms are basically different versions of PLL (Phase-locked loop) structures. They can be roughly divided into two groups, PLLs for single-phase converters and PLL algorithms for three-phase converters. For single-phase converters there are many existing structure and even dedicated ICs that can be used for such purpose. Three-phase converters are, on the other hand, quite different topic due to very specific requirements and quite complex, mostly due to different national grid code requirements.

2. PLL BASICS

Basic structure of the PLL is shown in Fig. 1. Such circuit is used in a wide range of applications, such as filtering, signal demodulation, clock multipliers and other synchronization purposes in digital electronics. In its simplest form, PLL consists of an input oscillating signal which is, along with the feedback signal, fed in to the phase detector circuit. Output of the phase detector circuit is filtered and passed into the output oscillator. Same signal is used as a feedback signal for the phase detector circuit.

For grid synchronization purposes, PLL structure is used differently. In this case, input of the structure is grid voltage at point *A*, and the output signal is taken from the integrator inside the VCO (Voltage controlled oscillator) at the point *B*. Output of the integrator represent a grid voltage phasor *angle* in 0-2π range.

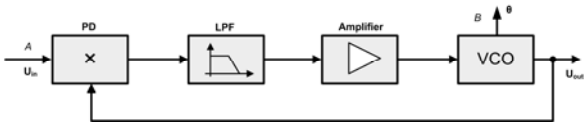

Fig. 1. *Basic PLL diagram*

3. VECTOR CONTROL

Phasor angle, extracted with a PLL circuit or estimated, is in case of the high-power grid-connected converters, necessary for converter control as most of the converters of this type use some form of vector control [1]. Most often, grid connected converters use some form of voltage oriented vector control (VOC) as shown in Fig. 2.

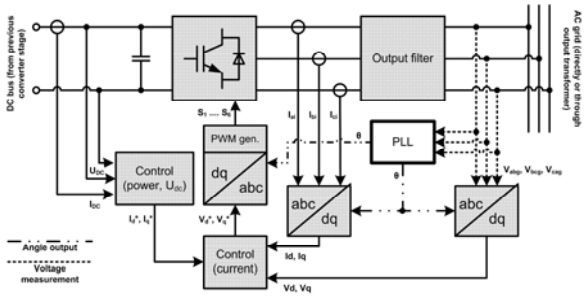

Fig. 2. *Block diagram of inverter VOC control*

As Fig. 2 shows, angle extracted using PLL structure plays vital role in performance of VOC controller, and therefore the inverter itself. Depending on the position of voltage sensor [13], or absence of it [5], PLL algorithm can be more or less complex.

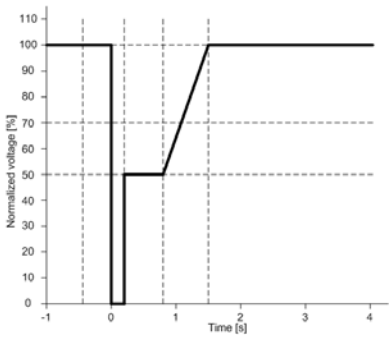

Fig. 3. *Sample waveform of grid voltage disturbance*

An added requirement for high-power converters is low voltage ride through (LVRT) capability [6],[7]. This requirement is not defined uniquely, but changes according to the national grid code requirements [10],[12]. Requirements deal with capability of inverter to survive grid disturbances and short circuits defined through voltage and its frequency at the grid connection point [8],[9]. Sample voltage profile is given in Fig. 3.

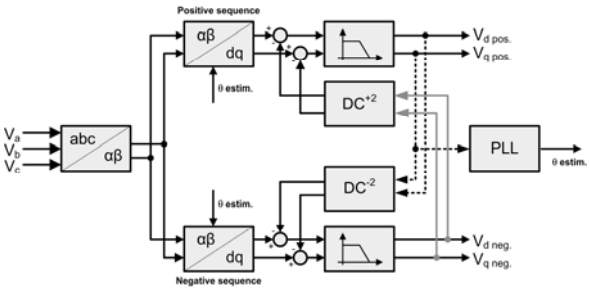

Fig. 4. *Block diagram of tested PLL structure*

Fig. 5. *Hardware in the loop system used for testing*

4. DEVELOPMENT AND TESTING

From many different existing PLL structures [2],[4],[11], focus was set on a decoupled double synchronous reference frame PLL (DDSRF-PLL) as literature [1],[3] shows its benefits over other structures. For in-depth evaluation of this structure, it has been compared with synchronous reference frame PLL structure (SRF-PLL). Also, as a baseline for both algorithms, grid angle extracted directly from measured voltages in αβ–frame was used.

Basic idea during the development was to accelerate the testing as much as possible, and implement the structure into the real converter without any major subsequent changes in the PLL structure, i.e. ready to run algorithm. For such requirement, PLL algorithm had to be fully tested with a range of disturbances as close as possible (and even worse) to those prescribed in grid codes and probable to occur in operation. On the other hand, the PLL algorithm had to be implemented on the system as close as possible to the target system, and the inverter had to be modelled appropriately. Therefore, a hardware-in-the-loop system, shown in the Fig. 5 coupled with DSP control board equal to the one used in the target inverter was used (DSP processor on the board is the same as the main DSP in target inverter on which the algorithms are implemented).

5. RESULTS

The PLL algorithm, in simplest form, was initially tested using the MATLAB/Simulink software, were both synchronization algorithms and grid with disturbances were modelled and algorithm results were compared with those on the proposed platform. Next, after the responses were verified, system was further developed and tested on the hardware in the loop system. The emulator was used for modelling grid and disturbances (and converter when needed), while the algorithms were programmed using programming tools and all DSP settings as those in the target converter. Responses are grouped according to the grid disturbance imposed on the PLL-s.

5.1. Voltage drops

Several different voltage drops were tested. First, symmetric voltage drops to 90%, 70% and 20% of the nominal grid voltage. The values selected for the testing are compilation of different grid code requirements [7], [10], but should give a correct insight for algorithm behaviour in converters for European countries. One reference result is shown in Fig. 6. The picture shows a voltage drop to approximately 45% of the nominal voltage. Element *VDN* is direct component of DDSRF positive rotating transformation, *OMEGADD* is estimated angular frequency taken from the same algorithm. Grid angles shown in the bottom are *PHISTDD* for DDSRF algorithm, *PHIST_H* for SRF algorithm and *PHIHMR* for grid angle taken directly measurements in αβ–frame. Same notation is used in the rest of the paper. From the results, it can be seen that all three algorithms, as expected, give the same results. Fig. 7 shows a component view of the symmetric voltage drop with voltage drop to 90% of nominal voltage. *VDN* and *VQN* are *D* and *Q* components of positive rotating transformation while *VDM* and *VQM* are inverse rotation

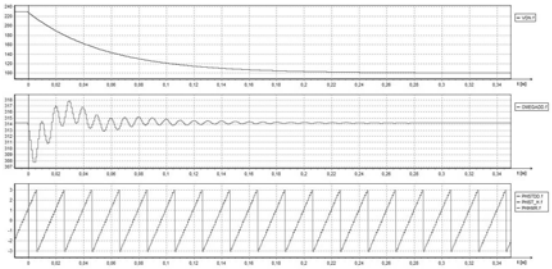

Fig. 6. *Symmetric voltage drops, from top: DDSRF direct D-component, estimated ω and grid angles.*

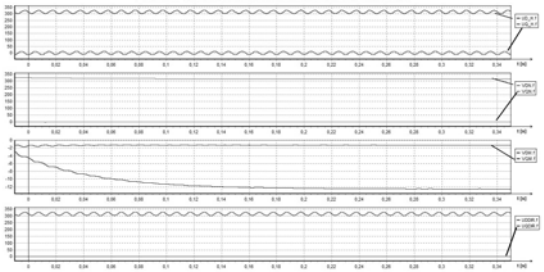

Fig. 7. *Symmetric voltage drops; from top: SRF components, DDSRF components, direct angle*

components. These and pictures further on are real-time recording from DSP system connected to the hardware-in-the-loop system. The expected behaviour of the system, i.e. minimum impact of the step change in amplitude on estimated angle in proposed algorithm was confirmed. After confirmation of system behaviour with symmetric voltage drops, asymmetric voltage drops (i.e. short circuits) of the same amount were applied to the PLL-s. For clearer view, the case for the voltage drop to 20% of the nominal voltage is shown in Fig. 8. Fig. 9 shows the same experiment, but in a longer time frame. Results show expected behaviour of synchronization structures, i.e. correct operation of DDSRF algorithm and oscillation of other structures which renders them inapplicable for our implementation.

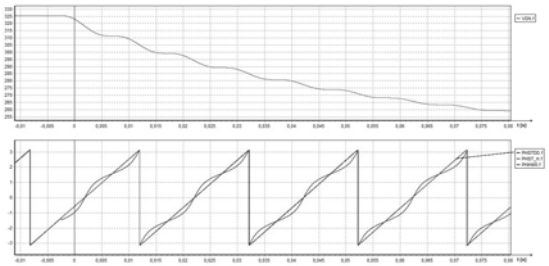

Fig. 8. *Asymmetric voltage drop (one phase); direct D component and phase outputs*

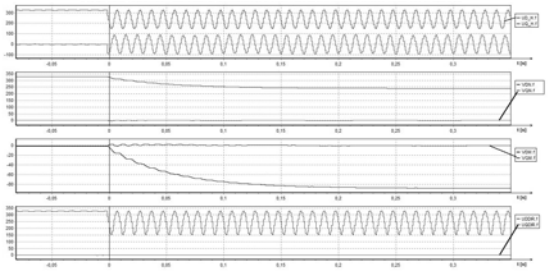

Fig. 9. *Asymmetric voltage drops; from top: SRF components, DDSRF components, direct angle*

5.2. Phase changes

Phase change in steps was selected heuristically to evaluate the algorithm behaviour, but no similar requirement exists in the grid codes. Phase was changed in all three phases for 5°, 15°, and 60° and even further, up to the 120°. The last value noted is actually equal to *phase skipping*. Such disturbance is highly unlikely to happen in practice but it is a usable tool to verify algorithm stability in extreme conditions. In special control algorithm implementations, disturbances similar to the simulated phase changes could occur in cases as, for instance, converter dropping into island mode or microgrid mode (loss of information on the actual grid angle) and connecting back to the grid (update of the grid voltage and angle). Results for smaller phase change are shown in Fig. 10 and Fig. 11. Results for extreme conditions are shown in Fig. 12 and Fig. 13. Results in Fig. 12 and Fig. 13 show that system output for grid angle expressed directly out of voltages in αβ–frame is completely erratic and therefore completely unusable. Results from the DDSRF algorithm, on the other hand, show that the system is unaffected by such disturbance. Also, from system responses shown it is clear that proposed algorithm can be even further fine-tuned.

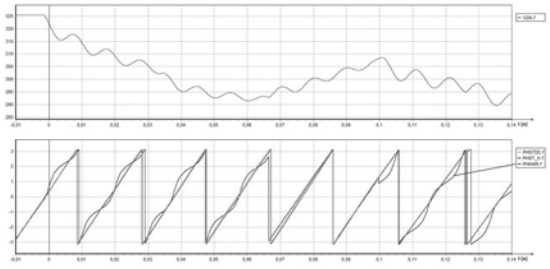

Fig. 10. *60 degree step change.*

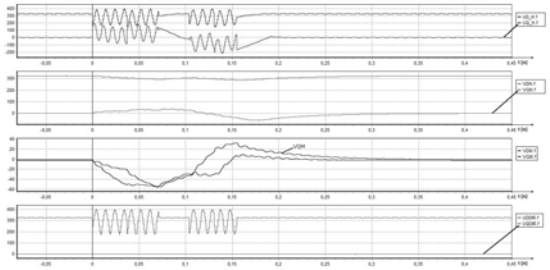

Fig. 11. *60 degree phase change; from top: SRF components, DDSRF components, direct angle*

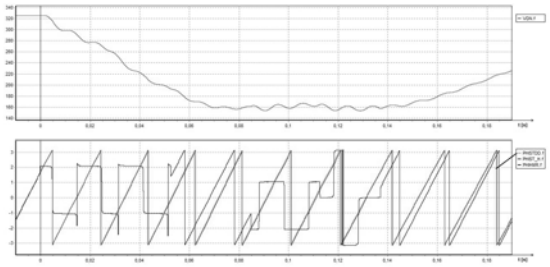

Fig. 12. *120 degree step change.*

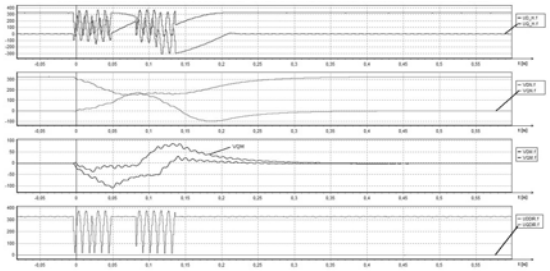

Fig. 13. *120 degree phase change; from top: SRF components, DDSRF components, direct angle*

5.3. Frequency changes

Included into the testing are also grid frequency step changes in reference to nominal 50Hz grid. For testing purposes, two extremes according to [6] were selected, changes to 47.5Hz and 51.5Hz. Fig. 14 shows, as in previous cases, grid angle outputs of all three systems and direct D component for DDSRF PLL.

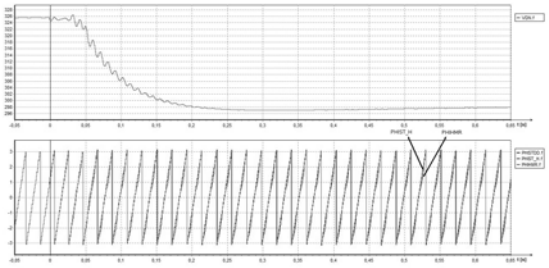

Fig. 14. *PLL response to step change in frequency from 50Hz to 47.5Hz*

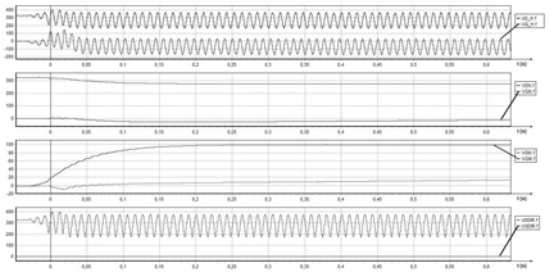

Fig. 15. *Frequency drop to 47.5Hz; from top: SRF components, DDSRF components, direct angle*

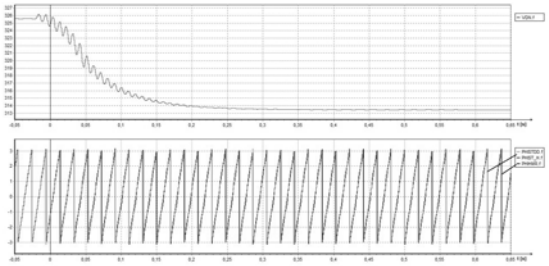

Fig. 16. *PLL response to step change in frequency from 50Hz to 51.5Hz*

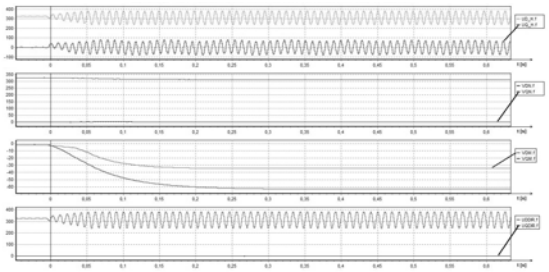

Fig. 17. *Frequency rise to 51.5Hz; from top: SRF components, DDSRF components, direct angle*

It can be seen that only DDSRF structure responds to such stimulus adequately. For better view, component view of all three systems is given in Fig. 15. In Fig. 16 and Fig. 17 are shown results of the same experiment, but now with increase of frequency to 51.5Hz. Again, only DDSRF behaviour is adequate. Moreover, by comparing Fig. 15 and Fig. 17, it can be seen that the disturbance can be assessed by examining *D* and *Q* components of direct and inverse transformations. In other words, the direction and amount of the frequency change can be measured and included in protection and supervisory logic of the converter controller.

5.4. Higher harmonic filtering

Special case for which the PLL algorithm was tested is operation in grid polluted with higher harmonics. Grid codes are not uniquely defined for such case and allowed harmonic content are often given explicitly in table form [7]. In some cases, this requirement is further defined implicitly as the maximum total harmonic distortion (THD) allowed. Specifically, a case was studied where grid voltage THD must be under 2.5% in case of the low-voltage grid [6]. This requirement is taken as the baseline for further development. It refers to the amount of harmonics that converter is allowed to inject into the grid, but it is also clear that it should operate without faults in grid with harmonic content up to this amount. Therefore, a synthetic voltage waveform as shown in Fig. 18 (top) was constructed and the PLL was tested using this waveform. It should be noted that such waveform is not usually found in the grid and can be considered the worst case for converter operation. Shown waveform qualitatively follows the allowed harmonic content arrangement as shown in [7], but for the clearer view, harmonics amplitudes were enlarged so that the waveform has THD much higher than required. As the results in Fig. 18 show, the behaviour of the PLL cannot be considered adequate. This problem is known and elaborated in the literature and several solutions are proposed [2]-[5]. Testing showed that some harmonics can be suppressed in DDSRF structure by fine tuning low-pass filters and PLL shown in Fig. 4, but this has worsened the system dynamics, as explained in [1] and could not be employed in specific implementation. As a possible solution, authors propose a pre-filtering structure based around the second-order generalized integrator (SOGI) shown in Fig. 19. Basic idea behind this proposal is for pre-filtering structure to, using its superior properties [1]-[5], suppresses higher harmonics, allowing the rest of the DDSRF structure to be optimized for required dynamics. Proposed structure is shown in Fig. 21, with mentioned SOGI structure and low-pass filters shaded. Fig. 20 shows the results of the modified structure in the same conditions as in Fig. 18

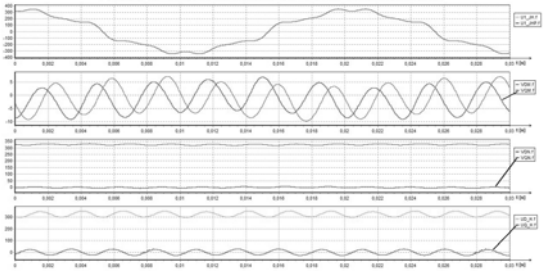

Fig. 18. *PLL behaviour in harmonics-polluted grid*

Fig. 19. *Schematic of second-order generalized integrator (SOGI)*

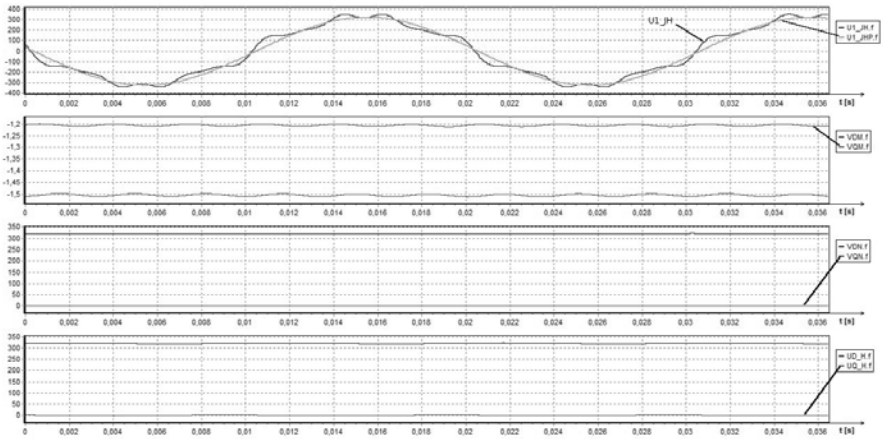

Fig. 20. *Response of modified PLL structure to harmonic polluted grid voltage*

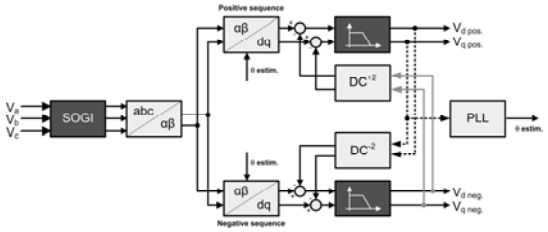

Fig. 21. *Modified DDSRF-PLL structure with added pre-filtering structure*

6. CONCLUSION AND FURTHER WORK

Results show that the implemented modified PLL structure is adequate for the high-power grid connected converter, i.e. for the converters on which the grid code requirements apply. The algorithm proved to be robust and precise, giving excellent results for asymmetries in the grid, as well as grid phase changes and voltage drops. Addition of pre-filter structure solved the main problem of the structure, the non-optimal performance when large quantities of higher harmonics are present in the grid. Used hardware in the loop system proved to be a valuable development tool as the modifications to the algorithm could be tested and implemented directly in the real-time system. Consequently, simulation times were cut down considerably and time consuming troubleshooting of problems related to the simulation software settings, were completely bypassed. For future work, proposed PLL structure found during development will be extensively tested on a real converter and benefits of the structure regarding dynamics, and its stability will be further analyzed theoretically.

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