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AC AND DC SIDE CURRENT RIPPLE CHARACTERISTICS OF THREE-PHASE NEUTRAL-POINT-CLAMPED THREE-LEVEL PWM INVERTERS

Özgür Bulut[1] **Ahmet M. Hava**[2]
Electrical-Electronics Engineering Department
Middle East Technical University
Çankaya, 06800 Ankara
ozgurblt@gmail.com[1] hava@metu.edu.tr[2]

Abstract: *The input and output current ripple characteristics of PWM operated three-phase neutral-point-clamped (NPC) three-level inverters, which directly determine the performance of the inverter, are thoroughly investigated. For each PWM method and operating point (modulation index M_i, power factor angle φ, carrier frequency f_c) there are unique input and output ripple current frequency spectrum characteristics. Thus, understanding, analysis, and design are challenging. This paper thoroughly investigates the high frequency ripple content of ac and dc side current spectral characteristics by using the equivalent centered harmonic (ECH) method. In addition, through detailed investigation, a clear understanding and quantification is provided about the low frequency harmonics of dc side current ripple causing mid-point potential variation. With this current spectral analysis, the input and output losses and mid-point voltage variation of three-phase NPC inverter are easily predicted. Thus; a better inverter, input capacitor, and output filter design is achieved. Furthermore, comparison with two-level inverter provides a conscious topology choice for the inverter designer.*

Keywords: ***AC Side Current Ripple, DC Side Current Ripple, Inverter, Mid-Point Voltage Variation, Neutral-Point-Clamped Inverters, PWM, Two-level Inverters***

1. INTRODUCTION

Three-phase three-level (3L) voltage source inverters (VSIs) are widely utilized in ac motor drives, uninterruptible power supplies (UPS), renewable energy systems, etc. to control the energy flow precisely, obtain high power quality and high energy efficiency. The neutral-point-clamped (NPC) VSI is the most commercially successful and developed 3L inverter topology (Fig. 1) used in industry and is favored over the two-level (2L) VSI in the high voltage/power applications [1]-[3]. Pulse-width-modulation (PWM) is the standard approach to operate the VSI switches in order to generate the required output voltages [3]-[5]. Of the various switching methods, this approach is mostly preferred due to the low-harmonic distortion waveform characteristics with well-defined harmonic spectrum, the fixed switching frequency (f_c), and implementation simplicity. Space vector or scalar (triangle intersection) implementation can be used, with the latter being easier to implement. Among the various scalar PWM methods existing (variety based on the zero sequence signal injection), space vector PWM (SVPWM) and discontinuous PWM (DPWM1) methods (the modulation waveforms of which are shown in Fig. 2) are popular due to their simplicity and performance advantages.

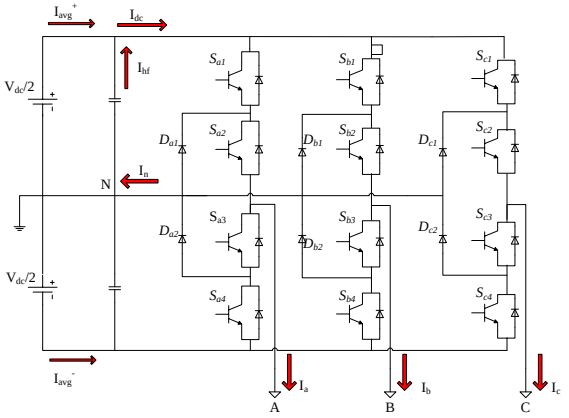

Fig. 1. *Three-phase 3L-NPC-VSI topology*

In the PWM approach, the desired VSI average output voltage is produced by making the magnitude and frequency of high frequency rectangular wave voltage pulses constant and adjusting their widths. Normally applied to loads with inductive filter characteristics (motors, utility grid, etc.), these voltages result in high frequency ripple content on the output current. In fact, this current ripple causes motor losses (core and copper) in motor drives, and creates torque ripple. In a PWM rectifier, filter inductors and capacitors take the ripple; therefore, losses and current/voltage ripple result. Due to the discrete nature of the inverter, eliminating the PWM voltage ripple is unavoidable; however, the output ripple current is unwanted and should be reduced as much as possible. The output PWM ripple voltage/current and their spectra depend

on the topology, PWM method, and modulation index, M_i ($M_i = \frac{V_{1m}}{\frac{2V_{dc}}{\pi}}$) [3]-[5]. The output ripple current and its spectra influence the inverter and motor design both from the peak stresses and losses perspective. Thus, it is important to obtain the output ripple current characteristics shaped by the PWM method and operating point (M_i) for an effective inverter design [6]. Similarly, ripple content of the dc-bus current bypassed through the dc-bus capacitor leads to capacitor losses (due to the capacitor equivalent series resistor (ESR) and/or dielectric losses), total dc-bus voltage ripple, and mid-point voltage variation for the 3L-NPC-VSI. The high frequency components (switching frequency and multiples) of the ripple current cause capacitor ESR losses and low frequency components (multiples of fundamental frequency) cause mid-point voltage variation which directly affects capacitor sizing. Therefore, the frequency spectra of the input and output ripple are highly important in analysis and design of 3L-NPC-VSI.

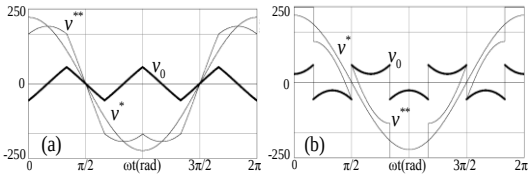

Fig. 2. *Modulation waveforms (v_x^{**}) and zero-sequence signals: left SVPWM right DPWM1 (M_i = 0.7) [1]*

The 2L-VSI input and output ripple characteristics are well investigated compared to 3L-NPC-VSI current ripple analysis. There is a lack of spectral current analysis of the 3L-NPC-VSI both for dc and ac side, considering the variety of PWM methods and number of parameters involved. In order to get a clear understanding of the input and output current spectrum characteristic of the 3L-NPC-VSI detailed study and comparison with 2L-VSI is needed. This paper provides some graphical and comparison tools to overcome this deficiency.

2. OUTPUT CURRENT RIPPLE CHARACTERIZATION OF 2L AND 3L VSI`S

In this section a detailed study is conducted in order to analyze the output current ripple of 3L-NPC-VSI and compare with the results of 2L-VSI. This analysis aids a clear understanding of the output current characteristics of 3L-NPC-VSI and makes a comparison with 2L-VSI. Simulation is done with 2L-VSI and 3L-NPC-VSI with an inductive (RL) load, using SVPWM and DPWM1 modulation methods. The fundamental frequency is 50 Hz for both inverters and the switching frequency is 6.6 kHz for SVPWM and 10 kHz for DPWM1 in order to equalize the switching losses. Additionally, in order to demonstrate the carrier frequency impact on the output current harmonics for the 3L-NPC-VSI, the same data has been taken with half of the switching frequency (of the 2L), i.e. 3.3 kHz for SVPWM and 5 kHz for DPWM1.

In Fig. 3, the total and dominant frequency current harmonic peak ($\text{rms} * \sqrt{2}$) values of 2L and 3L-NPC-VSIs for some critical operating points are graphed using the equivalent centered harmonic method (ECH). ECH lumps the harmonics at and around the carrier frequency to a single component (and likewise for the multiples of the carrier frequency) as illustrated in Fig. 4 [7] and by reducing the dimensions provides visual comprehension. Fig. 3 demonstrates both the total harmonic peak current and dominant harmonic ECH peak current. Therefore, the characteristic of the output current spectrum (total, dominant and other harmonics) of the 3L-NPC-VSI can be evaluated and compared it with the 2L-VSI. Another outcome of the study, Table 1 demonstrates that the most dominant harmonic frequency order (mD) is topology, PWM method, and M_i dependent. While for DPWM1 regardless the topology and M_i value, the dominant harmonics occur at f_c and side bands, for SVPWM the results highly vary significantly. It has been observed that generally the dominant harmonics are significantly larger than the other harmonics and for the performance evaluation and simple design purposes, the dominant harmonics could be sufficient to evaluate. Hence, using only the dominant harmonics provides an easier procedure.

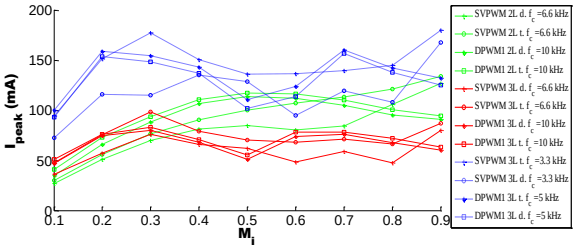

Fig. 3. *Total (t.) and dominant (d.) output current harmonics for different operating points of 2L-VSI and 3L-NPC-VSI*

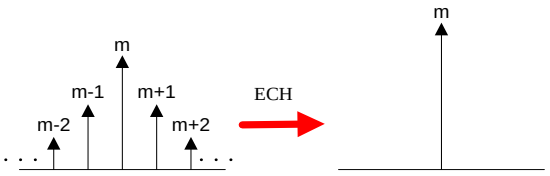

Fig. 4. *The equivalent centered harmonic representing the carrier frequency harmonic and its sidebands*

Considering the topologies and PWM methods together, 2L-VSI and 3L-NPC-VSI using SVPWM at f_c, DPWM1 at $1.5f_c$ (average switching frequency), and 3L-VSI using SVPWM at $f_c/2$ and DPWM1 at $0.75f_c$ (with f_c being 6.6 kHz) the comparison yields the following information.

First of all, the general usage of SVPWM and DPWM1 methods with 2L-VSI is as follows: at low M_i usage of SVPWM is much more common; on the other hand, at high M_i DPWM1 is favored. According to the Fig. 3, it can be clearly seen that SVPWM operated 2L-VSI generates less dominant and total harmonics for M_i < 0.6. However, DPWM1 operated 2L-VSI produces fewer harmonics for M_i more > 0.6. In addition dominant ECH locations of SVPWM operated 2L-VSI are at $2f_c$ at M_i less than 0.6 while they are at f_c at M_i higher than 0.6 (Table 1) which is an advantage for filter design. Hence, it is obvious for the 2L-VSI that SVPWM works better with low M_i while DPWM1 is better with high M_i.

Table 1. Output current dominant harmonic location of 2L and 3L VSIs for SVPWM and DPWM1 methods

	M_i	2L-VSI	3L-VSI
		mD	mD
SVPWM	0.1 – 0.2	2	2
	0.4 – 0.5	2	1
	0.6	2	2
	0.7 – 0.8	1	2
	0.9	1	1
DPWM1	0.1 - 0.9	1	1

The characteristics of the 3L-NPC-VSI output current harmonics to the operating conditions are different from 2L-

VSI. From Fig. 3 and Table 1 together, it can be seen that both the dominant and total harmonic current are approximately flat throughout the operating region, thus it is more appropriate to consider the total harmonic current for performance evaluation. Overall, in terms of output current harmonic ripple using DPWM1 at low M_i is better while SVPWM gives better results (less total harmonics, dominant harmonics at f_c) at high M_i 3L-NPC-VSI.

Compared to 2L-VSI, the overall harmonic content of 3L-NPC-VSI is lower for all the operating points (Fig. 3). Furthermore, the harmonic levels of 3L-NPC-VSI and 2L-VSI are close when switching frequency is half of the nominal, hence the switching frequency can be reduced by using the 3L-NPC-VSI (demonstrating the frequency multiplication effect).

3. DC SIDE CURRENT RIPPLE CHARACTERIZATION OF TWO AND THREE-LEVEL VSI

This section will investigate the dc bus ripple current characteristics of the 2L-VSI and 3L-NPC-VSI inverters via computer simulations and analytic calculations. Since 2L-VSI inverter is studied well, the focus will be placed on the 3L-NPC-VSI topology and its results will be presented and evaluated with respect to the 2L-VSI inverter characteristics reported in [7]. The twofold aspects of the dc side current are discussed in this section: the high frequency components resulting ripple on the dc bus current which cause thermal stresses and losses on the dc-bus capacitor both for 2L-VSI and 3L-NPC-VSI [7], and the low frequency part causing the 3L-NPC-VSI mid-point capacitor voltage variation. As a feature of the 3L-NPC-VSI, the mid-point of the VSI is connected to the neutral point (Fig. 1). Therefore, there is a current flow to the neutral point which is the reason of the mid-point voltage variation [9] - [11].

The dc side current of the 3L-NPC-VSI can be separated in three current branches. The positive side dc-bus current I_{avg}^{+}, the negative side dc-bus current I_{avg}^{-} and the neutral point I_n. These current waveforms are composed of picked fences changing with f_c, M_i, φ and PWM method (Fig. 5). I_{avg}^{+} and I_{avg}^{-} are same waveforms with a phase delay of 180˚. Therefore, investigation of I_{avg}^{+} and I_n is sufficient to obtain information about the dc side current. Since the dc bus capacitor takes the ripple of bus current, the high frequency current data is collected from I_{avg}^{+}. On the other hand, the low frequency data is needed to investigate the midpoint voltage variation; therefore, it is taken from I_n. The time domain data is not sufficient to give a clear understanding; therefore, the investigation is conducted on the frequency domain.

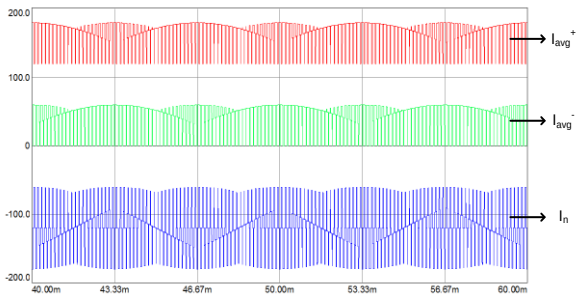

Fig. 5. *SVPWM operated 3L-NPC-VSI dc side currents: I_{avg}^{+}, I_{avg}^{-}, I_n (from top to the bottom) M_i=0.8; φ=0, I_{ph}=60A*

The dc-bus and neutral point current spectral contents are shown in Fig. 6 and 7 respectively. Figure 6 data is taken via simulating 2L and 3L-NPC-VSIs and Fig. 7 data is collected by simulating only the 3L-NPC-VSI, with switching frequency 6.6 kHz for SVPWM and 10 kHz for DPWM1 methods. The load is simulated as an ideal current source with 60A peak current with 50 Hz frequency.

The PWM method, M_i and φ are the fundamental parameters determining both the dc-bus high frequency harmonic current levels and dominant harmonic location of 3L-NPC-VSI as shown in Fig. 6 [8]. For example, in general the dominant harmonic of SVPWM operated 2L-VSI is at 2^{nd} multiple of f_c while the dominant harmonics of DPWM1 operated 2L-VSI and 3L-NPC-VSI are at the 1^{st} f_c (Table 2). A general observation shows that, the characteristic of SVPWM and DPWM1 operated 2L-VSI is similar such as at low φ and high M_i, and high φ and low M_i harmonics are lower. However, the dominant harmonics are at $2f_c$ for SVPWM operated 2L-VSI i.e. easier to filter [7]. SVPWM operated 3L-NPC-VSI brings out low harmonics when φ is high and M_i is too low or too high. The harmonics are lower for DPWM1 operated 3L-NPC-VSI when φ is high and M_i is in the middle of modulation range.

Table 2. *DC side current dominant harmonic location of 2L and 3L VSIs for SVPWM and DPWM1 methods*

		$f_{c\text{-}SVPWM}$ = 6.6kHz, $f_{c\text{-}DPWM1}$ = 10kHz		
Power Angle	**PWM Method**	**M_i**	**2L-VSI**	**3L-VSI**
			mD	**mD**
φ = 0, 30	SVPWM	0.1 – 0.9	2	1
	DPWM1	0.1 – 0.9	1	1
φ = 60	SVPWM	0.1 – 0.7	2	1
		0.8 – 0.9	1	1
	DPWM1	0.1 – 0.9	1	1
φ = 90	SVPWM	0.1	13	1
		0.2	7	1
		0.3 – 0.6	3	1
		0.7 – 0.8	1	2
		0.9	1	1
	DPWM1	0.1	9	5
		0.2	5	2
		0.3	3	2
		0.4	3	1
		0.5 – 0.6	2	1
		0.7 – 0.9	1	1

To sum up, the dc side current ripple is dependent to M_i, φ, PWM method and topology shown in Fig. 8. Not only the operating regions but also the trade-off relations define the topology and PWM method. For example, the dominant equivalent harmonics of 2L-VSI operating in SVPWM method are mostly at $2f_c$, or; DPWM method reduces switching losses, or for φ=90 the dominant harmonic location is very sensitive to M_i change. Although, there are some regions that 2L-VSI have better results, there are no significant difference between 3L-NPC-VSI harmonics. Moreover, by frequency multiplication effect 3L-NPC-VSI has lower switching losses with same ripple values. Considering the performance priorities and cost concerns the most appropriate topology and PWM method can be utilized. In addition, the total and dominant ripple current information can be obtained by the normalized current values in Fig. 6 and data in Table 2.

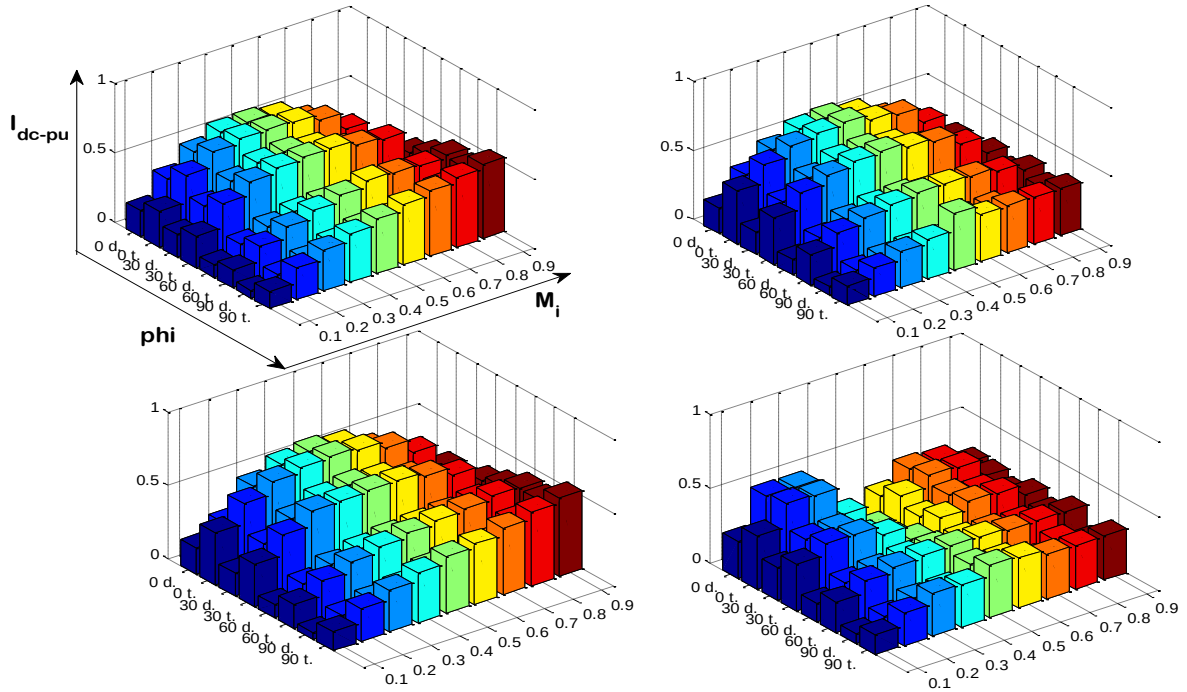

Fig. 6. *2L-VSI, 3L-NPC-VSI normalized dc-bus current ripple harmonics (d. most dominant, t. total harmonic at phi axis) top to the bottom: SVPWM, DPWM1 left to the right: 2L-VSI, 3L-NPC-VSI*

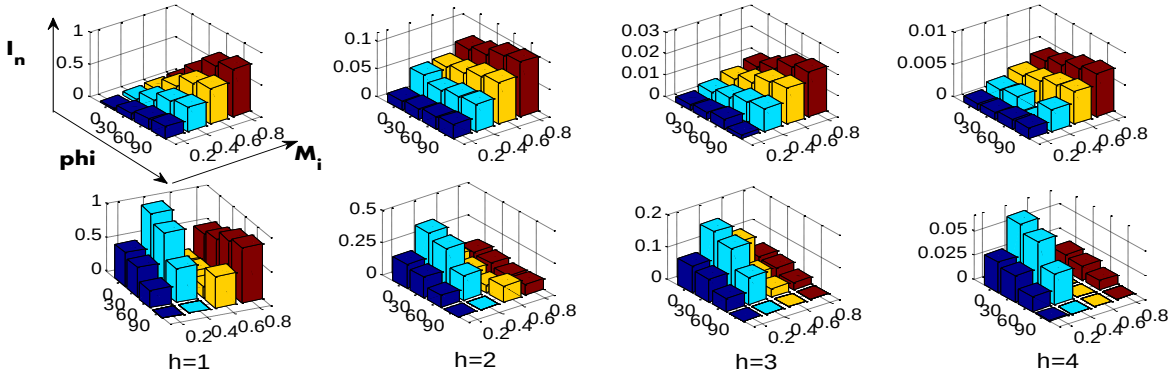

Fig. 7. *The normalized low frequency harmonics of 3L-NPC-VSI neutral current. From top to bottom: SVPWM, DPWM1. From left to right: first four harmonic peak values at f=150, 450, 750, 1050 Hz (h=1,2,3,4)*

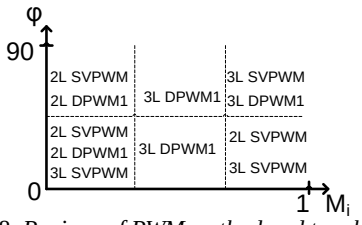

Fig. 8. *Regions of PWM method and topologies generating less dc side high frequency harmonics regions on the M_i vs. φ graph.*

As mentioned above, the structure of the 3L-NPC-VSI brings about a neutral current path called I_n (Fig. 1). Therefore, the neutral current is a switched part of the output current. This switched output current has both high and low frequency harmonics. The low frequency harmonics swing the midpoint capacitor voltage which causes a need for an additional balancing circuit and/or increased size of dc-bus capacitor.

The detailed analytical interpretation and analysis show that the neutral point low frequency harmonics are highly related to the injected zero sequence waveform; therefore, PWM method dependency. Figure 9 and 10 show the low-pass-filtered I_n, zero sequence signal and modulation signal to show the dependency and Fig. 11 demonstrates the time domain signals of midpoint voltage and neutral current. Furthermore, M_i and φ parameters effect the low frequency harmonics of neutral current since neutral current is a switched part of the output current (Fig. 7).

One of the major interpretation is that the low frequency harmonics are placed at $3(f_e + 2nf_e)$ due to the addition of three switched output current branches with 120˚phase difference. That means the first low frequency harmonic is at 150 Hz with 50 Hz fundamental frequency. This lowest harmonic is the dominant factor that effects the mid-point variation due to the capacitor impedance ($V = I/j\omega C$). The equivalent circuit of the dc-bus at harmonic frequencies contains two parallel bus capacitors; therefore the mid-point voltage variation can be calculated via (1). Using (1) along with Fig. 7 provides a powerful design tool to predict the mid-point voltage variation.

$$V = I_h/\omega_h C \qquad (1)$$

Figure 7 indicates that the first low frequency harmonic therefore the lowest mid-point variation occur low φ and low M_i for SVPWM method. For DPWM1 method, power factor angle response of the low frequency harmonics differs with M_i due to the discontinuous characteristic of the modulation wave (Fig. 2). At low M_i, low φ brings out lower harmonics and at high M_i vice versa. In general SVPWM method brings out much less low frequency harmonics than DPWM1 method. However as φ increase the DPWM1 method becomes more usable. SVPWM method is better at low φ and low M_i and DPWM1 method is better at high φ and low M_i. Overall, as the harmonic levels at Fig. 7 and the time domain signals shown in Fig. 11 show that the major part that determine the mid-point voltage variation is the first harmonic of I_n.

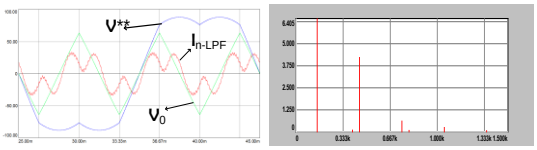

Fig. 9. *3L-NPC-VSI low-pass-filtered mid-point current($I_{n\text{-}LPF}$) (left: time domain, right: frequency domain), zero sequence signal (V_0) and modulation waveform (V^{**}) for SVPWM M_i=0.8; φ=0, I_{ph}=60A*

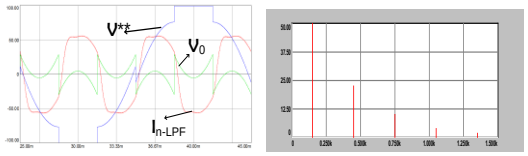

Fig. 10. *3L-NPC-VSI low-pass-filtered mid-point current($I_{n\text{-}LPF}$) (left: time domain, right: frequency domain), zero sequence signal (V_0) and modulation waveform (V^{**}) for DPWM1 M_i=0.8, φ=0, I_{ph}=60A*

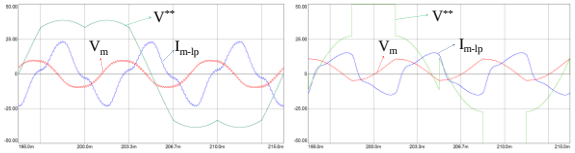

Fig. 11. *3L-NPC-VSI midpoint voltage (V_m) and low-pass-filtered midpoint current ($I_{m\text{-}lp}$) and modulation waveform (V^{**}) (left:SVPWM method, right: DPWM1 method, M_i=0.7, φ=30)*

The voltage ripple on the dc-bus capacitor is one of the main parameters to determine the capacitor sizing. Figure 7 shows the normalized current values of I_n. Using equation (1), the voltage ripple, therefore the capacitor choice can be easily made for different inverter applications.

4. CONCLUSION

This paper has focused on the input and output current ripple characteristic of the 3L-NPC and compared it with 2L-VSI results. The high frequency spectral characteristic of input and output current is established via a simple approximation method, equivalent centered harmonic approach. The low frequency harmonics of midpoint current harmonics are shown for different operating points to help a better understanding of the mid-point current characteristic. Centered dominant harmonics and total harmonics are shown in a 2D graph for 2L and 3L VSIs for different operating points which serve to designer a reasonable choice with lower output current ripple. The input line current total and dominant centered harmonics are put in a 3D graph which is a powerful design tool to choose a proper size dc-bus capacitor. The first few harmonics of the midpoint current are presented in another 3D graph so that the midpoint voltage swing can easily be predicted.

This paper additionally suggests commonly used PWM methods for different operating points for various VSI applications with better output current ripple, dc-bus current ripple and midpoint voltage swing performance. To sum up, the output ripple current performance of 2L-VSI is better with SVPWM at low M_i, and DPWM with high M_i while 3L-NPC-VSI gives better results with DPWM method at low M_i and SVPWM at high M_i. In addition, the effective operating points are well summarized in Fig. 8 for the dc-bus high frequency ripple of 2L-VSI and 3L-NPC-VSI. The neutral current of the 3L-NPC-VSI has a much lower low frequency harmonic content with SVPWM operation and the method to predict the voltage swing of the midpoint is presented. With the help of the study in this paper, a better 3L-NPC-VSI and dc bus capacitor design can be achieved.

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