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"Differential Power"

-A metric to compare and optimize power converters and architectures-

***Abstract*—** Recent improvements in GaN and SiC power switches move the focus to the reactive components, which need to be minimized to reduce volume and cost of power architectures. "Differential Power", which is the minimum "internal, indirect, or ac power" needed to be processed by the reactive components of a power converter, is a high-level metric very useful to compare, design and optimize power converters and power architectures, with special impact on the size and losses. One example is energy buffered converters, as those required in single-phase inverters connected to domestic batteries/PV panels or those required in Power Factor Correction applications. Another thrilling example are hybrid converters, which include inductors in traditional switched cap architectures to achieve soft-charging of the capacitors and therefore improve dramatically efficiency and reduce size.

This methodology is illustrated through the participation of the team CEI@UPM in the "Little Box Challenge" (Google and IEEE-PELS) and the design of high power/high voltage resonant switched capacitors. The talk begins with an overview of several projects and activities developed for Industry partners at CEI-UPM.

Tutorial Content:

1 Motivation. High level metric to compare power architectures

2 Basics of Power conversion:

2.1 Inductor based vs capacitor based power converters
2.2 Hybrid converters
2.3 Gain & regulation

3 Fundamental limits of Power Conversion

3.1 Historical review
3.2 Related concepts: "Partial Power" and "Differential Power converters"
3.3 Direct, Indirect & Differential Power

4 How to calculate "Direct" and "Differential" Power at:

4.1 Circuit/Topological level
4.2 Converter & System level: "Averaged Power Model"

5 Case studies, at power converter level

5.1 Buck, Boost, Buck-boost

5.2 Two-input Buck
5.3 3-level Buck
5.4 Z-source converter

6 Case studies, at power architecture level

6.1 Step-up and step-down converters
6.2 Cascaded and stacked converters
6.3 Energy Buffered architectures. Power unbalance
6.4 Fundamental limits of Energy Buffered architectures: the "3-port Average power model"
6.5 Comparison of architectures
6.6 Single-stage inverter operating in the Fundamental limit

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José A. Cobos is a Full Professor at the Universidad Politécnica de Madrid and Chair of the "Industrial Council @ CEI". He lectures Electronics with special focus on Fundamentals, Analog, and Power Electronics, for Undergraduate, Master and Doctoral students.

His contributions are focused in the field of power supply systems for telecom, aerospace, industrial, automotive, renewable energy and medical applications. His research interests include energy efficiency in digital systems and RF amplifiers, magnetic components, piezoelectric transformers, transcutaneous energy transfer and dynamic power management. He also works in the generation of EM fields for water supercooling and biomedical effects. He advised over 40 Master Thesis and 14 Doctoral dissertations, published over 50 journal papers and over 300 technical papers, and holds 8 patents. He conducted professional seminars and tutorials in USA, UK, Austria, Germany, Italy, Sweden, Switzerland, Syria, Mexico and Macedonia.

in 2006, he was the founder Director of the "Centro de Electrónica Industrial, CEI-UPM", a University research center leading a strong industrial program in power electronics and digital systems. In 2016, he was the founder President of the "Industrial Council @ CEI" to coordinate Education & Research with Industry, and provide scholarships to CEI students, sponsored by Airbus S&D – CRISA, Thales Alenia Space, Bosch, Premo, Huawei, Indra, Ansys, Viesca, Airbus and Apex. He has been RCC Fellow at Harvard University and recipient of a Fulbright grant to work on Energy Efficiency, at UC Berkeley.